200ball FBGA Specification

16Gb LPDDR4 (x32)

1. FEATURES

[LPDDR4]

· VDD1 = 1.8V (1.7V to 1.95V)

· VDD2, VDDCA and VDDQ = 1.1V (1.06 to 1.17)

· VSSQ terminated DQ signals (DQ, DQS_t, DQS_c, DMI)

· Single data rate architecture for command and address;
- all control and address latched at rising edge of the clock

· Double data rate architecture for data Bus;
- two data accesses per clock cycle

· Differential clock inputs (CK_t, CK_c)

· Bi-directional differential data strobe (DQS_t, DQS_c)
  - Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)

· DMI pin support for write data masking and DBIdc functionality

· Programmable RL (Read Latency) and WL (Write Latency)

· Burst length: 16 (default), 32 and On-the-fly
  - On the fly mode is enabled by MRS

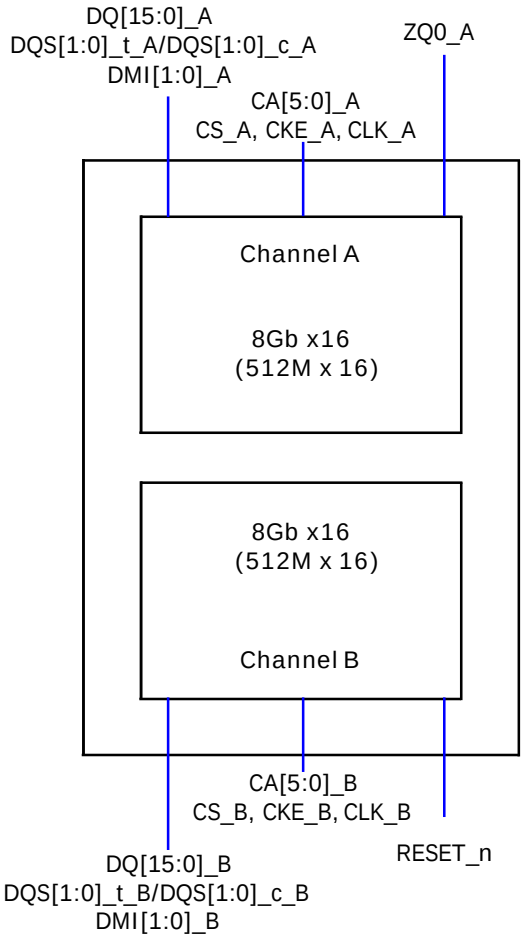
· Auto refresh and self refresh supported
· All bank auto refresh and directed per bank auto refresh supported

· Auto TCSR (Temperature Compensated Self Refresh)

· PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask

· Background ZQ Calibration

Functional Block Diagram



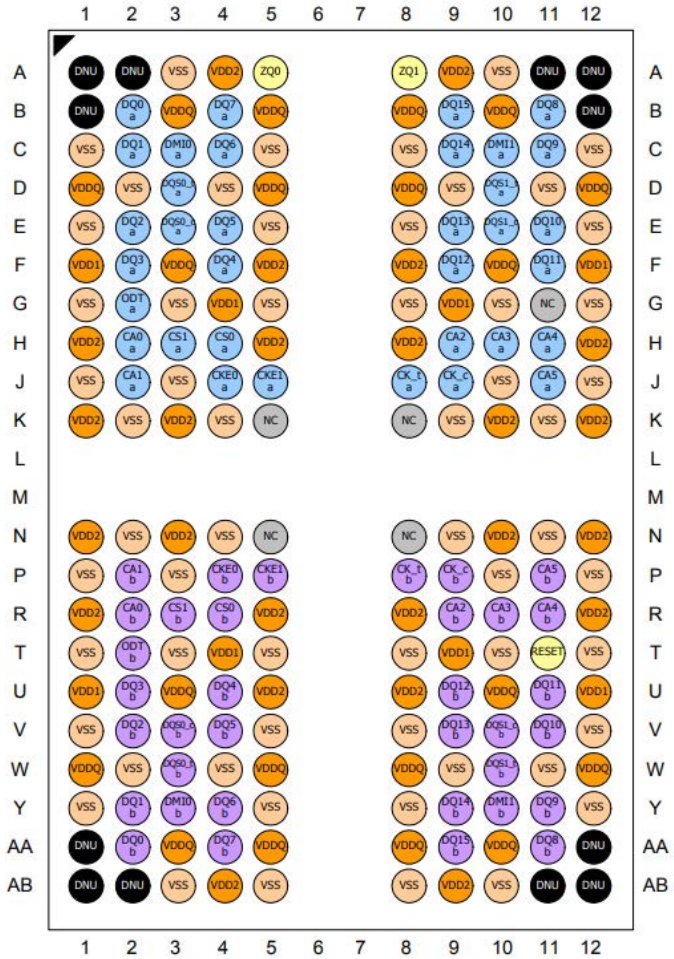
ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
DM4H16GCMNDI4-B4	LPDDR4	1.8V/1.1/1.1	16Gb (x16, 2Channel)	DDR4 2400	200Ball FBGA (Lead & Halogen Free)
DM4H16GCMNDI4-B6	LPDDR4	1.8V/1.1/1.1	16Gb (x16, 2Channel)	DDR4 2666	200Ball FBGA (Lead & Halogen Free)
DM4H16GCMNDI4-C2	LPDDR4	1.8V/1.1/1.1	16Gb (x16, 2Channel)	DDR4 3200	200Ball FBGA (Lead & Halogen Free)

2. Package ballout & Addressing

2.1. FBGA package

2.1.1. 200 balls, 10x15mm^2, 0.8 x 0.65mm pitch



Top View

200ball LPDDR4 (2CH) only

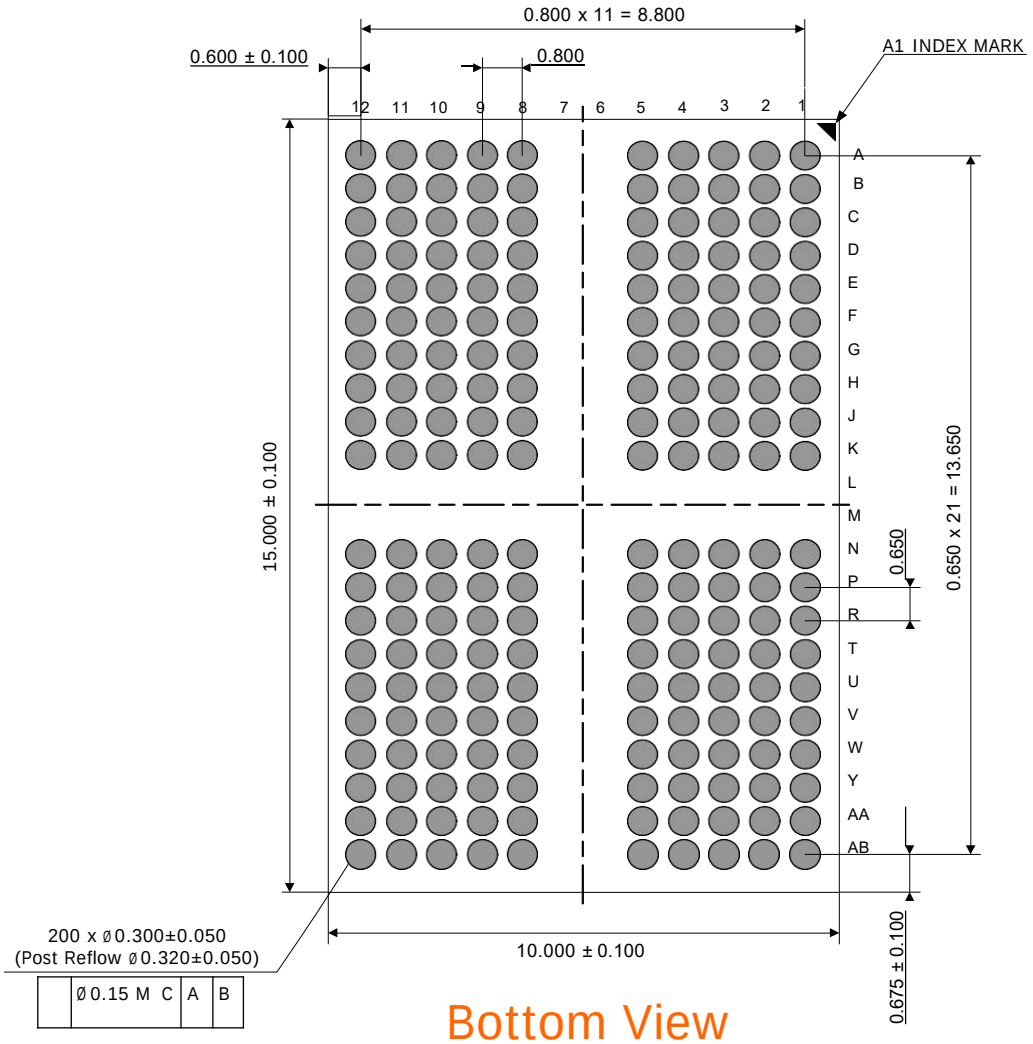
LPDDR4 Channel a
LPDDR4 Channel b
Power (VDD1,VDD2,VDDCA,VDDQ,VREF)
Ground (VSS,VSSCA,VSSQ)

Notes:

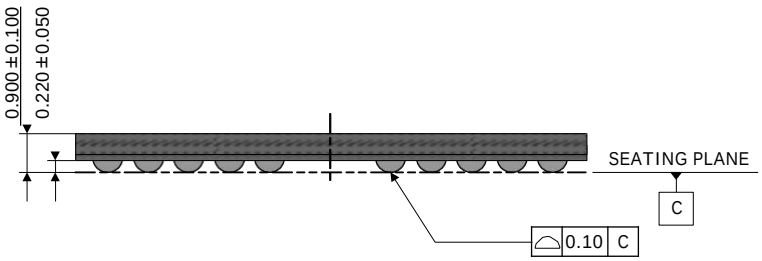
1. 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows
2. Top View, A1 in top left corner
3. ODT_CA_[x] balls are wired to ODT_CA)_[x] pads of Rank 0 DRAM die. The ODT input to other rank (if present) will be connected to VSS in the package.
4. ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC

2.2. Mechanical specification

200 Ball 0.65/0.80mm pitch 10.00mm x 15.00mm FBGA *[t = 1.00mm max]*



Bottom View



Front View

2.3. Pin Description

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are refer- enced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5 0]_B	Input	Command/Address Inputs: Provide the Command and Address in- puts according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output : Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_ B DQS[1:0]_c_ B	I/O	Read Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center aligned with Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOWwhen the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Eachchan- nel (A & B) has its own DMI signals.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240-Ω ± 1% resistor.
VDD1, VDD2, VDDQ	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS	GND	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.

3. Functional Description

LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured as an 2-channel memory with 8-bank memory per each channel.

These devices contain the following number of bits per die:
4Gb has 4,294,967,296 bits
6Gb has 6,442,450,944 bits
8Gb has 8,589,934,592 bits
12Gb has 12,884,901,888 bits
16Gb has 17,179,869,184 bits
24Gb has 25,769,803,776 bits
32Gb has 34,359,738,368 bits

LPDDR4 devices use multi cycle of single data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address and bank information. Each command uses two clock cycles, during which command information is transferred on positive edge of the corresponding clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation

3.1. LPDDR4 SDRAM Addressing

Memory Density (per Die)		4Gb	6Gb	8Gb	12Gb	16Gb
Memory Density (per channel)		2Gb	3Gb	4Gb	6Gb	8Gb
Configuration		16 Mb x 16 DQ x 8 banks x 2 channels	24 Mb x 16 DQ x 8 banks x 2 channels	32 Mb x 16 DQ x 8 banks x 2 channels	48Mb x 16DQ x 8 banks x 2 channels	64 Mb x 16 DQ x 8 banks x 2 channels
Number of Channels per die		2	2	2	2	2
Number of Banks per Channel		8	8	8	8	8
Array Pre-fetch (bits, per channel)		256	256	256	256	256
Number of Rows per Channel		16,384	24,576	32,768	49,152	65,536
Number of Columns (fetch boundaries)		64	64	64	64	64
Page Size (Bytes)		2048	2048	2048	2048	2048
Channel Density (Bits per channel)		2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592
Total Density (Bits per die)		4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184
Bank Address		BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2
x16	Row Addresses	R0 - R13	R0 – R14 (R13=0 when R14=1)	R0 - R14	R0 – R15 (R14=0 when R15=1)	R0 - R15
	Column Addresses	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9
Burst Starting Address Boundary		64-bit	64-bit	64-bit	64-bit	64-bit

1. The lower two column addresses (C0-C1) are assumed to be "zero" and are not transmitted on the CA bus.
2. Row and Column address values on the CA bus that are not used for a particular density are "don't care."
3. For non-binary memory densities, only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

3.2. Simplified State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

Figure - Simplified State Diagram

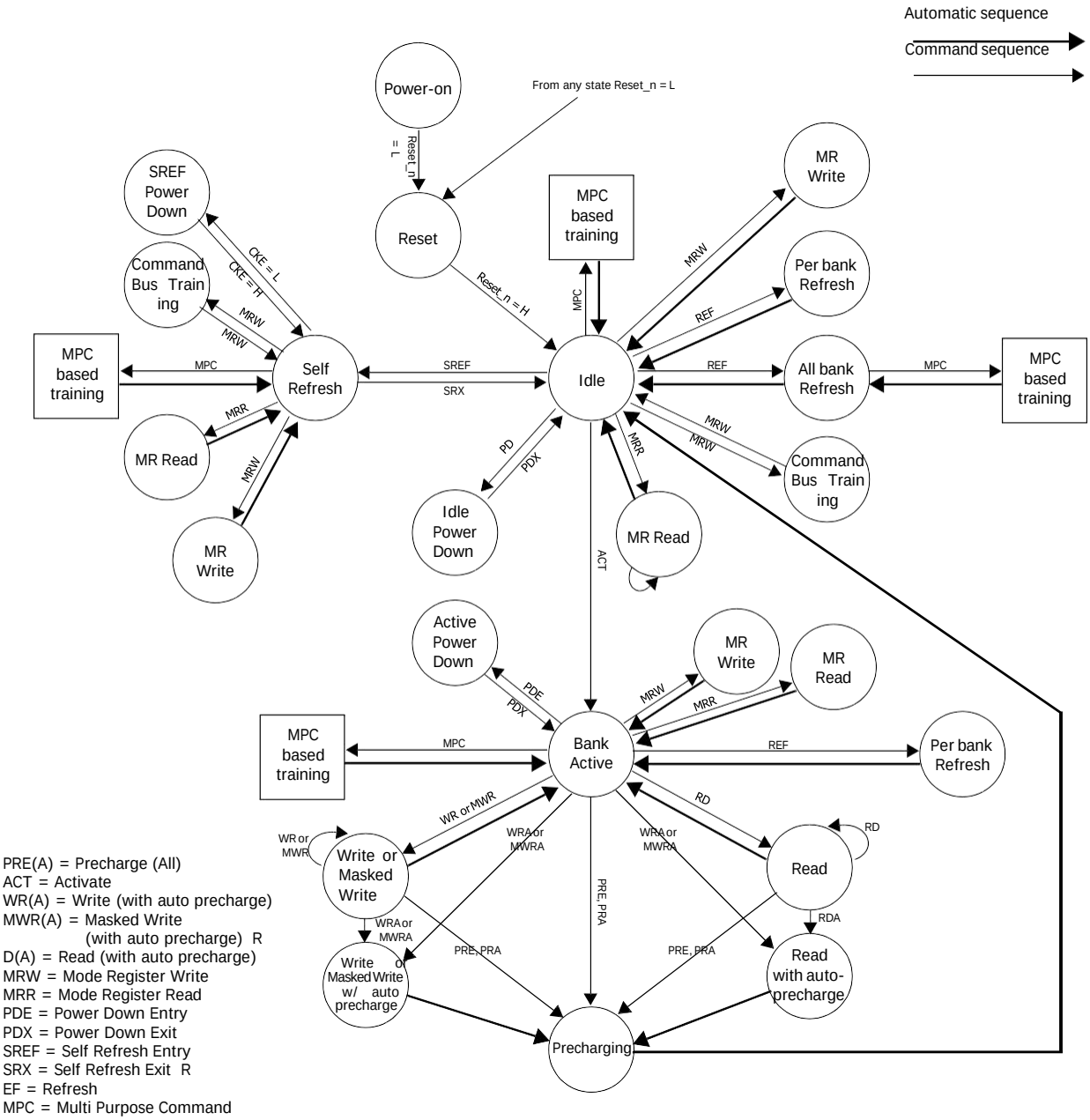
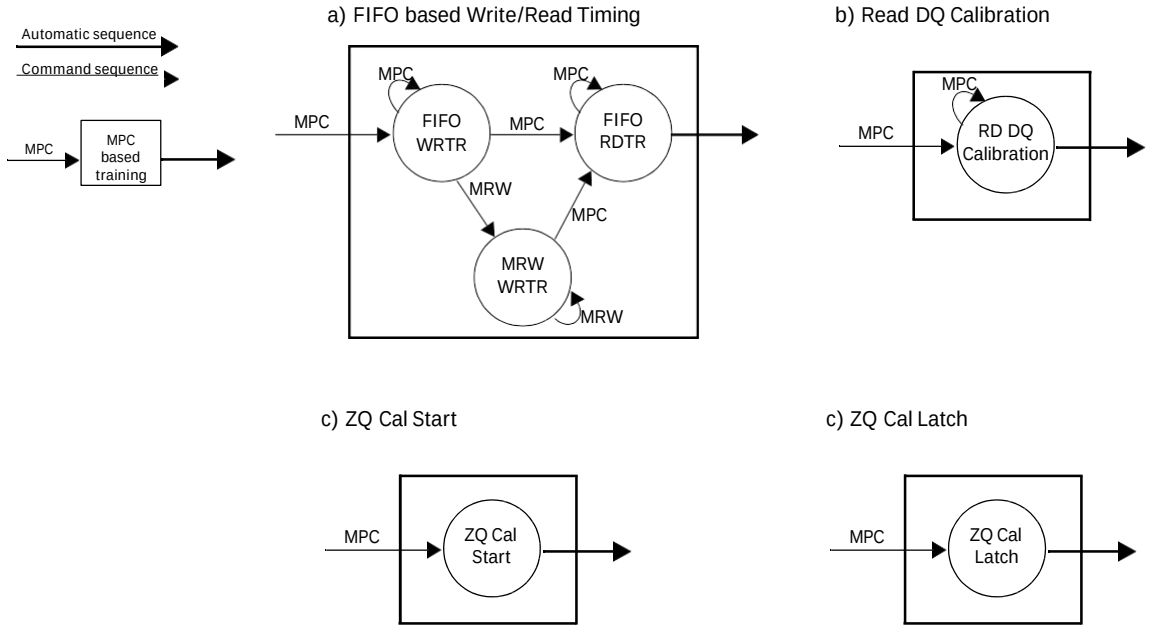


Figure - Simplified Bus Interface State Diagram



Notes:

1. From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2. In IDLE state, all banks are pre-charged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

3.2.1. Power-up and Initialization

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as following table.

Table - MRS defaults settings

Item	MRS	Default setting	Description
FSP-OP/WR	MR13 OP[7:6]	00B	FS-OP/WR[0] are enabled
WLS	MR2 OP[6]	0B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000B	WL = 4
RL	MR2 OP[2:0]	000B	RL = 6, nRTP = 8
nWR	MR1 OP[6:4]	000B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000B	DQ ODT is disabled
Vref(ca) Setting	MR12 OP[6]	1B	Vref(ca) Range[1] enabled
Vref(ca) value	MR12 OP[5:0]	001101B	Range1: 27.2% of VDDQ
Vref(DQ) Setting	MR14 OP[6]	1B	Vref(DQ) Range[1] enabled
Vref(DQ) Value	MR14 OP[5:0]	001101B	Range1: 27.2% of VDDQ

3.2.1.1. Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDD2) and all inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table "Voltage Ramp Conditions". VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table - Voltage Ramp Conditions

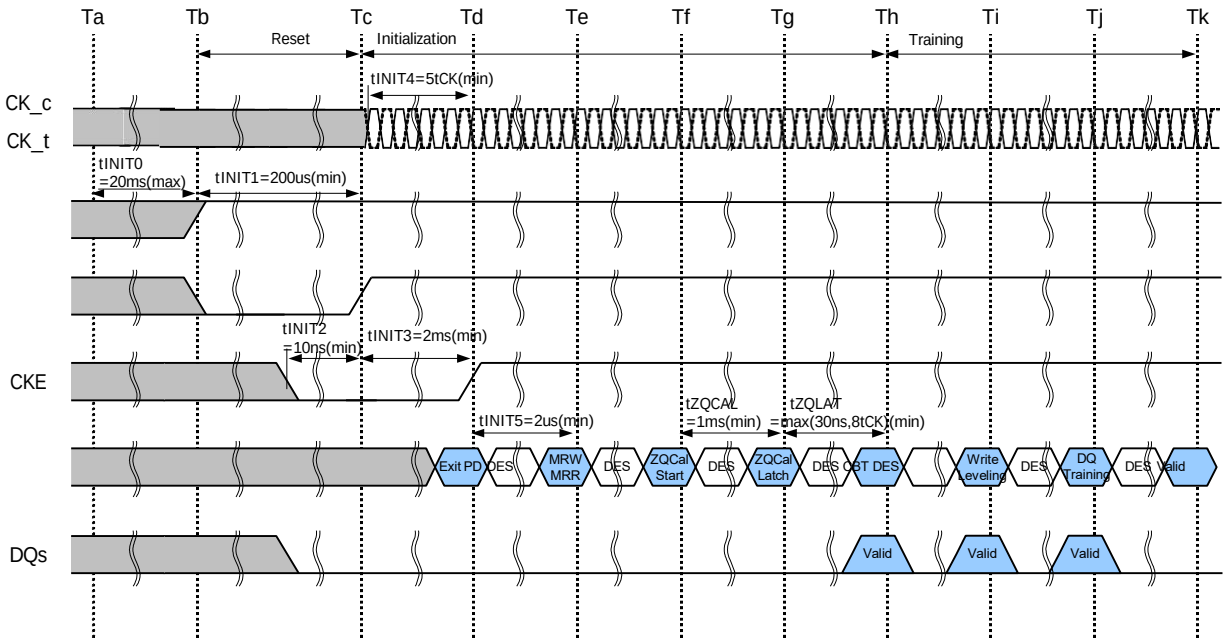
After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

Note:
1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
5. The voltage difference between any of VSS and VSSQ pins must not excess 100mV.

2.Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between Vss and VDD2 during voltage ramp to avoid latch-up.

3.Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

Figure - Power Ramp and Initialization Sequence



Note

1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch(Th, Sequence7~9) in the above figure, is simplified recommendation and actual training sequence may vary depending on systems.

4.After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK_t,CK_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.

5.After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6.After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7.After tZQLAT is satisfied (Th) the command bus (internal VREF(ca), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and VREF(ca) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.
The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter

exit the training mode.

8.After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high(Ti). See write leveling section for detailed description of write leveling entry and exit sequence . In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.

9.After write leveling, the DQ Bus (internal VREF(dq), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(dq)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and VREF(dq) set to a default factory setting. Normal device oper- ation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

8.At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more reg- isters that have not previously been set up for normal operation should be written at this time.

Table - Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0		20	ms	Maximum Voltage Ramp Time
tINIT1	200		us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10		ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2		ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5		tCK	Minimum stable clock before first CKE HIGH
tINIT5	2		us	Minimum idle time before first MRW/MRR command
tCKb	Note 1, 2	Note 1, 2	ns	Clock cycle time during boot

Notes
1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

3.2.1.2. Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.
1.Assert RESET_n below 0.2 x VDD2 anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n.

2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

Table - Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100	-	ns	Minimum RESET_n low time for Reset Initialization with stable power

3.2.2.Power-off Sequence

3.2.2.1.Controlled Power-off

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤0.2 X VDD2) and all other inputs must be between VILmin and VIH max. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

Table - Power Supply Conditions for Power-off

Between...	Applicable Conditions
TX and TZ	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200mV

Note: The voltage difference between any of VSS, VSSQ pins must not exceed 100mV

3.2.2.2. Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/ µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table - Timing Parameters for Power-off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF		2	s	Maximum Power-off ramp time

3.3. Mode Register Definition

Table below shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Reg- ister Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table. Mode Register Assignment

MR#	MA <5:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Information	R	CATR	RFU		RZQI		RFU		Refresh Mode	MR0
1	01H	Device Feature 1	W	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL		MR1
2	02H	Device Feature 2	W	WR Lev	WLS	WL			RL			MR2
3	03H	IO Configuration 1	W	DBI-WR	DBI-RD	PDDS			RFU	WR-PST	PU-CAL	MR3
4	04H	Refresh Rate	R/W	TUF	RFU		PPRE	RFU	Refresh Rate			MR4
5	05H	Basic Configuration 1	R	LPDDR4 Manufacturer ID								MR5
6	06H	Basic Configuration 2	R	Revision ID-1								MR6
7	07H	Basic Configuration 3	R	Revision ID-2								MR7
8	08H	Basic Configuration 4	R	IO Width		Density			Type			MR8
9	09H	Test Mode	W	Vendor Specific Test Mode								MR9
10	0AH	ZQ Reset	W	RFU							ZQ Reset	MR10
11	0BH	ODT Feature	W	RFU	CA ODT			RFU	DQ ODT			MR11
12	0CH	VREF(ca) R0	R/W	RFU	VR-CA	VREF(ca)						MR12
13	0DH	Functional options	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT	MR13
14	0EH	VREF(dq)	R/W	RFU	VR(dq)	VREF(dq)						MR14
15	0FH	Invert Register 0	W	Lower Byte Invert for DQ Calibration								MR15
16	10H	PASR Bank	W	PASR Bank Mask								MR16
17	11H	PASR Segment	W	PASR Segment Mask								MR17
18	12H	DQS Oscillator 1	R	DQS Oscillator Count - LSB								MR18
19	13H	DQS Oscillator 2	R	DQS Oscillator Count - MSB								MR19
20	14H	Invert Register 1	W	Upper Byte Invert for DQ Calibration								MR20
21	15H	Vendor Specific	N/A	RFU								MR21
22	16H	SOC ODT Feature	W	RFU		ODTD-CA	ODTE-CS	ODTE-CK	CODT			MR22
23	17H	DQS Oscillator Run Time	W	DQS Oscillator Run Time Setting								MR23
24	18H	TRR	R/W	TRR	TRR Bank Address			U-MAC	MAC Value			MR24
25	19H	PPR Resource	R	Post Package Repair Resources								MR25
26:31	1AH:1FH	RFU	N/A	Reserved for Future Use								
32	20H	DQ Calibration - Pattern A	W	See "DQ Calibration" section								MR32
33:39	21H:27H	DNU	N/A	Do Not Use								
40	28H	DQ Calibration - Pattern B	W	See "DQ Calibration" section								MR40
41:47	29H:2FH	DNU	N/A	Do Not Use								
48:63	30H:3FH	RFU	N/A	Reserved for Future Use								

1. RFU bits should be set to '0' during mode register writes
2. RFU bits should be read as '0' during mode register reads

3. All mode registers that are specified as RFU or Write-only shall return undefined data when read and DQS_t/DQS_c shall be toggled
4. All mode registers that are specified as RFU shall not be written
5. See vendor device datasheet for details on vendor-specific mode registers
6. Writes to Read-only registers shall have no effect on the functionality of the device

3.3.1. MR0 Register Information (MA[5:0] = 00H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CATR	RFU		RZQI		RFU		Refresh Mode

Function	Register Type	Operand	Data	Notes
Refresh Mode	Read-only	OP[0]	0B: Both legacy & modified refresh mode supported 1B: Only modified refresh mode supported	
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00B: RZQ Self-Test Not Supported 01B: ZQ pin may connect to VSS or float 10B: ZQ-pin may short to VDDQ 11B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to VDD2 or float, nor short to VSS)	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	0B: CA for this rank is not terminated 1B: CA for this rank is terminated	

Notes:
1. RZQI, if supported, will be set upon the completion of the MRW ZQ Initialization Calibration command.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected
3. to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate might indicate a ZQ-pin assembly error. It is recommend ed that the assem- bly error is corrected.
4. In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will
5. ignore ZQ Calibration commands. In either case, the device may not function as intended.
6. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result
7. cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).
8. OP[7] is set at power-up, according to the state of the CA-ODT pad on the die AND the state of MR11 OP[7]. If the CAO DT pad is tied LOW, then the die will not terminate the CA bus and MR12 OP[7]=0B, regardless of the state of ODTECA
9. (MR11 OP[7]). If
   the CA-ODT pad is tied HIGH AND ODTE-CA is enabled (MR11 OP[7]=1B), then this bit will be set (MR0 OP[7]=1B) and the die
   will terminate the CA bus.

3.3.2. MR1 Register Information (MA[5:0] = 01H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Register Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00B: BL=16 Sequential (default) 01B: BL=32 Sequential 10B: BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1,5,6
WR-PRE (WR Pre-amble Length)		OP[2]	0B: Reserved 1B: WR Pre-amble = 2nCK (default)	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0B: RD Pre-amble = Static (default) 1B: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto Precharge commands)		OP[6:4]	000B: nWR = 6 (default) 001B: nWR = 10 010B: nWR = 16 011B: nWR = 20 100B: nWR = 24 101B: nWR = 30 110B: nWR = 34 111B: nWR = 40	2,5,6
RPST (RD Post-amble Length)		OP[7]	0B: RD Post-amble = 0.5*tCK (default) 1B: RD Post-amble = 1.5*tCK	4,5,6

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the "BL" bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. See Table, "Frequency Ranges for RL , WL, and nWR Settings" later in this section
3. For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" pre-amble. See the preamble section for a drawing of each type of pre-amble.
4. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.3.2.1. Burst Sequence

Table - Burst Sequence for Read

Burst Length	Burst Type	C4	C3	C2	C1	Co	Burst Cycle Number and Burst Address Sequence																																					
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																						
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																						
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																						
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																						
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Burst Length	Burst Type	C4	C3	C2	C1	Co	Burst Cycle Number and Burst Address Sequence																																					
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																						
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

1. C1:C0 input is not present on CA bus. It is implied zero.
2. The starting burst address is on 64-bit (4n) boundaries.
3. C2-C3 for BL16 and C2-C4 for BL32 shall be set to '0' for all Write operations.

3.3.3. MR2 Register Information (MA[5:0] = 02H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WR Lev	WLS	WL			RL		

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write only	OP[2:0]	DBI Disable (MR3 OP[6]=0B) 000B: RL= 6 & nRTP = 8 (Default) 001B: RL= 10 & nRTP = 8 010B: RL= 14 & nRTP = 8 011B: RL= 20 & nRTP = 8 100B: RL= 24 & nRTP = 10 101B: RL= 28 & nRTP = 12 110B: RL= 32 & nRTP = 14 111B: RL= 36 & nRTP = 16 DBI Enable (MR3 OP[6]=1B) 000B: RL= 6 & nRTP = 8 001B: RL= 12 & nRTP = 8 010B: RL= 16 & nRTP = 8 011B: RL= 22 & nRTP = 8 100B: RL= 28 & nRTP = 10 101B: RL= 32 & nRTP = 12 110B: RL= 36 & nRTP = 14 111B: RL= 40 & nRTP = 16	1,3,4
WL (Write latency)		OP[5:3]	**Set "A" (MR2** OP[6]=0B) 000B: WL=4 (Default) 001B: WL=6 010B: WL=8 011B: WL=10 100B: WL=12 101B: WL=14 110B: WL=16 111B: WL=18 **Set "B" (MR2 OP[6]=1B)** 000B: WL=4 001B: WL=8 010B: WL=12 011B: WL=18 100B: WL=22 101B: WL=26 110B: WL=30 111B: WL=34	1,3,4
WLS (Write latency set)		OP[6]	0B: WL Set "A" (default) 1B: WL Set "B"	1,3,4
WR Lev (Write Leveling)		OP[7]	0B: Disabled (default) 1B: Enabled	2

1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR operand, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR operand, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.3.3.1. Read and Write Latencies (Frequency Ranges for RL, WL, and nWR Settings)

Read Latency		Write Latency		nWR	nRTP	Freq. limit (Greater than)	Freq. limit (Same or less than)	Notes
No DBI	w/ DBI	Set **"A"**	Set **"B"**					
6	6	4	4	6	8	10	266	1,2,3,4,5,6
10	12	6	8	10	8	266	533	
14	16	8	12	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	
nCK	*nCK*	*nCK*	*nCK*	*nCK*	*nCK*	*MHz*	*MHz*	

Notes:
1. The LPDDR4-SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3-OP[6]. When MR3-OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3-OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set "A" and Set "B" is determined by MR2-OP[6]. When MR2-OP[6]=0, then Write Latency Set "A" should be used. When MR2-OP[6]=1, then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Read burst with AP (auto-pre-charge) enabled. It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a pre-charge.

3.3.4. MR3 Register Information (MA[5:0] = 03H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	PDDS			RFU	WR-PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-CAL (Pull-up Calibration Point)	Write only	OP[0]	0B: VDDQ/2.5 1B: VDDQ/3 (default)	1,4
WR-PST (Write Post-amble length)		OP[1]	0B: WR Post-amble = 0.5*tCK (default) 1B: WR Post-amble = 1.5*tCK (Vendor Specific)	2,3,5
PDDS (Pull-down Drive Strength)		OP[5:3]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0B: Disabled (default) 1B: Enabled	2,3
DBI-WR (DBI-WR Enable)		OP[7]	0B: Disabled (default) 1B: Enabled	2,3

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. PU-CAL setting is required as the same value for both Ch.A and Ch.B before ZQCAL start command.
5. DLI 8Gb LPDDR4 doesn't require 1.5*tCK apply => 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

3.3.5. MR4 Register Information (MA[5:0] = 04H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	RFU		PPRE	RFU	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000B: SDRAM Low temperature operating limit exceeded 001B: 4x refresh 010B: 2x refresh 011B: 1x refresh (default) 100B: 0.5x refresh 101B: 0.25x refresh, no-rating 110B: 0.25x refresh, with de-rating 111B: SDRAM High temperature operating limit exceeded	1,2,3,4, 7,8,9

Function	Register Type	Operand	Data	Notes
PPRE (Post-package repair entry/ exit)	Write	OP[4]	0B: Exit PPR mode (default) 1B: Enter PPR mode	5,9
TUF (Temperature Update Flag)	Read	OP[7]	0B: No change in OP[2:0] since last MR4 read (default) 1B: Change in OP[2:0] since last MR4 read	6,7,8

1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. If OP[2]=0B, the device temperature is less or equal to 85℃. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1, the device temperature is greater than 85℃.
2. At higher temperatures (>85℃), AC timing de-rating may be required. If de-rating is required the LPDDR4-SDRAM will set OP[2:0]=110B. See de-rating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000B or 111B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7]=0 at power-up. OP[2:0] bits are undefined at power-up.
8. See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4.
9. OP[6:3] bits are that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register

3.3.6. MR5 Register Information (MA[5:0] = 05H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR4 Manufacturer ID							

Function	Register Type	Operand	Data	Notes
LPDDR4 Manufacturer ID	Read-only	OP[7:0]	00000110B : SK hynix	

3.3.7. MR6 Register Information (MA[5:0] = 06H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-1	Read-only	OP[7:0]	00000000B: A-version 00000001B: B-version	1

1. Please contact DLI office for MR6 code for this device.

3.3.8. MR7 Register Information (MA[5:0] = 07H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-1	Read-only	OP[7:0]	00000000B: A-version 00000001B: B-version	1

1. Please contact DLI office for MR7 code for this device.

3.3.9. MR8 Register Information (MA[5:0] = 08H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width		Density				Type	

Function	Register Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00B: S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000B: 4Gb per die (2Gb per channel) 0001B: 6Gb per die (3Gb per channel) 0010B: 8Gb per die (4Gb per channel) 0011B: 12Gb per die (6Gb per channel) 0100B: 16Gb per die (8Gb per channel) 0101B: 24Gb per die (12Gb per channel) 0110B: 32Gb per die (16Gb per channel) All Others: Reserved	
IO Width		OP[7:6]	00B: x16 (per channel) All Others: Reserved	

3.3.10. MR9 Register Information (MA[5:0] = 09H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

1. Only 00H should be written to this register.

3.3.11. MR10 Register Information (MA[5:0] = 0AH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							ZQ Reset

Function	Register Type	Operand	Data	Notes
ZQ Reset	Write-only	OP[0]	OB: Normal Operation (Default) 1B: ZQ Reset	1,2

1. See the AC Timing tables for calibration latency and timing
2. If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

3.3.12. MR11 Register Information (MA[5:0] = 0BH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA ODT			RFU	DQ ODT		

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	0000B: Disable (Default) 0001B: RZQ/1 0010B: RZQ/2 0011B: RZQ/3 0100B: RZQ/4 0101B: RZQ/5 0110B: RZQ/6 0111B: RFU	1,2,3

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the register s for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.3.13. MR12 Register Information (MA[5:0] = 0CH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR-CA	VREF(ca)					

Function	Register Type	Operand	Data	Notes
VREF(ca) (VREF(ca) Setting)	Read/Write	OP[5:0]	000000B: -- Thru – 110010B: See table below All Others: Reserved	1,2,3,5,6
VREF(ca) Range		OP[6]	0B: VREF(ca) Range[0] enabled 1B: VREF(ca) Range[1] enabled (default)	1,2,4,5,6

1. This register controls the VREF(ca) levels for Frequency-Set-Point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting OP[6] appropriately.
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(ca) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(ca) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(ca) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(ca) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(ca) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table - VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR12	OP[5:0]	000000B: 10.0%	011010B: 20.4%	000000B: 22.0%	011010B: 32.4%	1,2,3
		000001B: 10.4%	011011B: 20.8%	000001B: 22.4%	011011B: 32.8%	
		000010B: 10.8%	011100B: 21.2%	000010B: 22.8%	011100B: 33.2%	
		000011B: 11.2%	011101B: 21.6%	000011B: 23.2%	011101B: 33.6%	
		000100B: 11.6%	011110B: 22.0%	000100B: 23.6%	011110B: 34.0%	
		000101B: 12.0%	011111B: 22.4%	000101B: 24.0%	011111B: 34.4%	
		000110B: 12.4%	100000B: 22.8%	000110B: 24.4%	100000B: 34.8%	
		000111B: 12.8%	100001B: 23.2%	000111B: 24.8%	100001B: 35.2%	
		001000B: 13.2%	100010B: 23.6%	001000B: 25.2%	100010B: 35.6%	
		001001B: 13.6%	100011B: 24.0%	001001B: 25.6%	100011B: 36.0%	
		001010B: 14.0%	100100B: 24.4%	001010B: 26.0%	100100B: 36.4%	
		001011B: 14.4%	100101B: 24.8%	001011B: 26.4%	100101B: 36.8%	
		001100B: 14.8%	100110B: 25.2%	001100B: 26.8%	100110B: 37.2%	
		001101B: 15.2%	100111B: 25.6%	001101B: 27.2% (Default)	100111B: 37.6%	
		001110B: 15.6%	101000B: 26.0%	001110B: 27.6%	101000B: 38.0%	
		001111B: 16.0%	101001B: 26.4%	001111B: 28.0%	101001B: 38.4%	
		010000B: 16.4%	101010B: 26.8%	010000B: 28.4%	101010B: 38.8%	
		010001B: 16.8%	101011B: 27.2%	010001B: 28.8%	101011B: 39.2%	
		010010B: 17.2%	101100B: 27.6%	010010B: 29.2%	101100B: 39.6%	
		010011B: 17.6%	101101B: 28.0%	010011B: 29.6%	101101B: 40.0%	
		010100B: 18.0%	101110B: 28.4%	010100B: 30.0%	101110B: 40.4%	
		010101B: 18.4%	101111B: 28.8%	010101B: 30.4%	101111B: 40.8%	
		010110B: 18.8%	110000B: 29.2%	010110B: 30.8%	110000B: 41.2%	
		010111B: 19.2%	110001B: 29.6%	010111B: 31.2%	110001B: 41.6%	
		011000B: 19.6%	110010B: 30.0%	011000B: 31.6%	110010B: 42.0%	
		011001B: 20.0%	All Others: Reserved	011001B: 32.0%	All Others: Reserved	

1. These values may be used for MR12 OP[5:0] to set the VREF(ca) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

3.3.14. MR13 Register Information (MA[5:0] = 0DH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPRE-TR	CBT

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write	OP[0]	0B: Normal Operation (default) 1B: Command Bus Training mode enabled	1
RPRE-TR (Read Preamble Training)		OP[1]	0B: Normal Operation (default) 1B: Read Preamble Training mode enabled	
VRO (Vref Output)		OP[2]	0B: Normal Operation (default) 1B: Output the Vref(ca) value on DQ[0] and the Vref(dq) value on DQ[1]	2
VRCG (VREF Current Generator)		OP[3]	0B: Normal Operation (default) 1B: VREF Fast Response (high current) mode	3
RRO (Refresh Rate Option)		OP[4]	0B: Disable MR4 OP[2:0] (default) 1B: Enable MR4 OP[2:0]	4,5
DMD (Data Mask Disable)		OP[5]	0B: Data Mask Operation Enabled (default) 1B: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write Enable)		OP[6]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point[1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point[1]	8

1. A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the VREF(ca) training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the VREF(ca) training section for more information.
2. When set, the LPDDR4-SDRAM will output the VREF(ca) voltage on DQ[0] and the VREF(dq) voltage on DQ[1]. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4 devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), Masked Write Command is not allowed and it is illegal. See the Data Mask section for more information.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions: Vref(CA) Setting, Vref(CA) Range, Vref(DQ) Setting, Vref(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ
   Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following func- tions: Vref(CA) Setting, Vref(CA) Range, Vref(DQ) Setting, Vref(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.

3.3.15. MR14 Register Information (MA[5:0] = 0EH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR(dq)	VREF(dq)					

Function	Register Type	Operand	Data	Notes
VREF(dq) Setting for Set Point[0]	Read / Write	OP[5:0]	000000B: -- Thru – 110010B: See table below All Others: Reserved	1,2,3,4,5,6
VREF(dq) Range		OP[6]	0B: VREF(dq) Range[0] enabled 1B: VREF(dq) Range[1] enabled (default)	1,2,3,4,5,6

1. This register controls the VREF(dq) levels for Frequency-Set-Point[1:0]. Values from either VR(dq)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(dq) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(dq) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(dq) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(dq) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(dq) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table - VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR14	OP[5:0]	000000B: 10.0%	011010B: 20.4%	000000B: 22.0%	011010B: 32.4%	1,2,3
		000001B: 10.4%	011011B: 20.8%	000001B: 22.4%	011011B: 32.8%	
		000010B: 10.8%	011100B: 21.2%	000010B: 22.8%	011100B: 33.2%	
		000011B: 11.2%	011101B: 21.6%	000011B: 23.2%	011101B: 33.6%	
		000100B: 11.6%	011110B: 22.0%	000100B: 23.6%	011110B: 34.0%	
		000101B: 12.0%	011111B: 22.4%	000101B: 24.0%	011111B: 34.4%	
		000110B: 12.4%	100000B: 22.8%	000110B: 24.4%	100000B: 34.8%	
		000111B: 12.8%	100001B: 23.2%	000111B: 24.8%	100001B: 35.2%	
		001000B: 13.2%	100010B: 23.6%	001000B: 25.2%	100010B: 35.6%	
		001001B: 13.6%	100011B: 24.0%	001001B: 25.6%	100011B: 36.0%	
		001010B: 14.0%	100100B: 24.4%	001010B: 26.0%	100100B: 36.4%	
		001011B: 14.4%	100101B: 24.8%	001011B: 26.4%	100101B: 36.8%	
		001100B: 14.8%	100110B: 25.2%	001100B: 26.8%	100110B: 37.2%	
		001101B: 15.2%	100111B: 25.6%	001101B: 27.2% (Default)	100111B: 37.6%	
		001110B: 15.6%	101000B: 26.0%	001110B: 27.6%	101000B: 38.0%	
		001111B: 16.0%	101001B: 26.4%	001111B: 28.0%	101001B: 38.4%	
		010000B: 16.4%	101010B: 26.8%	010000B: 28.4%	101010B: 38.8%	
		010001B: 16.8%	101011B: 27.2%	010001B: 28.8%	101011B: 39.2%	
		010010B: 17.2%	101100B: 27.6%	010010B: 29.2%	101100B: 39.6%	
		010011B: 17.6%	101101B: 28.0%	010011B: 29.6%	101101B: 40.0%	
		010100B: 18.0%	101110B: 28.4%	010100B: 30.0%	101110B: 40.4%	
		010101B: 18.4%	101111B: 28.8%	010101B: 30.4%	101111B: 40.8%	
		010110B: 18.8%	110000B: 29.2%	010110B: 30.8%	110000B: 41.2%	
		010111B: 19.2%	110001B: 29.6%	010111B: 31.2%	110001B: 41.6%	
		011000B: 19.6%	110010B: 30.0%	011000B: 31.6%	110010B: 42.0%	
		011001B: 20.0%	All Others: Reserved	011001B: 32.0%	All Others: Reserved	

1. These values may be used for MR14 OP[5:0] to set the VREF(dq) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

3.3.16. MR15 Register Information (MA[5:0] = 0FH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Lower Byte Invert for DQ Calibration	Write	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
1. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
2. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table - MR15 Invert Register Pin Mapping

Pin	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	No-invert	OP4	OP5	OP6	OP7

3.3.17. MR16 Register Information (MA[5:0] = 10H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Bank Mask							

Function	Register Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0B: Bank Refresh enabled (default) : Unmasked 1B: Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank masking is on a per channel basis. The two channels on the die may have different bank masking.

3.3.18. MR17 Register Information (MA[5:0] = 11H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write-only	OP[7:0]	0B: Segment Refresh enabled (default) 1B: Segment Refresh disabled	1

Seg-ment	OP[n]	Seg-ment Mask	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	TBD	TBD
0	0	xxxxxxx1	000B						
1	1	xxxxxx1x	001B						
2	2	xxxxx1xx	010B						
3	3	xxxx1xxx	011B						
4	4	xxx1xxxx	100B						
5	5	xx1xxxxx	101B						
6	6	x1xxxxxx	110B	Not Allowed	110B	Not Allowed	110B	Not Allowed	110B
7	7	1xxxxxxx	111B		111B		111B		111B

1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.
3. For 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00B).

3.3.19. MR18 Register Information (MA[5:0] = 12H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscilla-tor)	Read-only	OP[7:0]	0:255 LSB DRAM DQS Oscillator Count	1,2,3

1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS t o the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

3.3.20. MR19 Register Information (MA[5:0] = 13H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0:255 MSB DRAM DQS Oscillator Count	1,2

1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

3.3.21. MR20 Register Information (MA[5:0] = 14H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Upper Byte Invert for DQ Calibration	Write	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1,2

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's . Ex- ample: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
1. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
2. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table - MR20 Invert Register Pin Mapping

Pin	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	No-invert	OP4	OP5	OP6	OP7

3.3.22. MR21 Register Information (MA[5:0] = 15H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Mode Registor							

3.3.23. MR22 Register Information (MA[5:0] = 16H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration	Write	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non-terminating rank)		OP[3]	0B: ODT-CK Over-ride Disabled (Default) 1B: ODT-CK Over-ride Enabled	2,3,4,6,8
ODTE-CS (CS ODTenable for non-terminating rank)		OP[4]	0B: ODT-CS Over-ride Disabled (Default) 1B: ODT-CS Over-ride Enabled	2,3,5,6,8
ODTD-CA (CA ODT termination disable)		OP[5]	0B: ODT-CA Obeys ODT_CA bond pad (default) 1B: ODT-CA Disabled	2,3,6,7,8

Notes:
1. All values are "typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.
5. When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.
6. For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.
7. When OP[5]=0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT_CA bond pad or MR11-OP[6:4].
8. To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22

or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down and Precharge Power-down.

3.3.24. MR23 Register Information (MA[5:0] = 17H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS oscillator run time setting							

Function	Register Type	Operand	Data	Notes
DQS oscillator run time	Write	OP[7:0]	00000000B: DQS timer stops via MPC Command (Default) 00000001B: DQS timer stops automatically at 16th clocks after timer start 00000010B: DQS timer stops automatically at 32nd clocks after timer start 00000011B: DQS timer stops automatically at 48th clocks after timer start 00000100B: DQS timer stops automatically at 64th clocks after timer start ---------- Thru ---------- 00111111B: DQS timer stops automatically at (63X16)th clocks after timer start 01XXXXXXB: DQS timer stops automatically at 2048th clocks after timer start 10XXXXXXB: DQS timer stops automatically at 4096th clocks after timer start 11XXXXXXB: DQS timer stops automatically at 8192nd clocks after timer start	1, 2

3.3.25. MR24 Register Information (MA[5:0] = 18H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TRR Mode	TRR Mode Bank Address			Unlimited MAC	MAC Value		

Function	Register Type	Operand	Data	Notes
MAC Value	Read	OP[2:0]	000B: Unknown when bit OP3 =0 (note 1) Unlimited when bit OP3=1 (note 2) 001B: 700K 010B: 600K 011B: 500K 100B: 400K 101B: 300K 110B: 200K 111B: Reserved	
Unlimited MAC		OP[3]	0B: OP[2:0] define MAC value 1B: Unlimited MAC value (note 2, note 3)	
TRR Mode BAn	Write	OP[6:4]	000B: Bank 0 001B: Bank 1 010B: Bank 2 011B: Bank 3 100B: Bank 4 101B: Bank 5 110B: Bank 6 111B: Bank 7	
TRR Mode		OP[7]	0B: Disabled (default) 1B: Enabled	

Note:
1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

3.3.26. MR25 Register Information (MA[5:0] = 19H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Function	Register Type	Operand	Data	Notes
PPR Resource	Read	OP[7:0]	0B: PPR Resource is not available 1B: PPR Resource is available	

3.3.27. MR26:31 Register Information (MA[5:0] = 1AH:1FH)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved							

3.3.28. MR32 Register Information (MA[5:0] = 20H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "A" (default = 5AH)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	XB: An MPC command with OP[6:0]=0000011B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5AH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	

3.3.29. MR33:39 Register Information (MA[5:0] = 21H:27H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Do Not Use							

3.3.30. MR40 Register Information (MA[5:0] = 28H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B" (default = 3CH)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	XB: A default pattern "3CH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3,4

Notes:
1. The pattern contained in MR40 is contatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR22 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

4. Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.5	V	1
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.5	V	1
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

Notes:
1. See the section "Power-up, Initialization, and Power-off" for information about relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, please refer to JESD51-2 standard.

5. AC and DC Operating Conditions

5.1. Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Core Power 1	VDD1	1.70	1.80	1.95	V	1,2
Core Power 2 & CA Power	VDD2	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	VDDQ	1.06	1.10	1.17	V	2,3

1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mV at the DRAM ball is not included in the TdIVW.

5.2. Operating Temperature

Parameter		Symbol	Min	Max	Unit	Note
Operating Temperature	Standard	T_{OPER}	0	85	°C	1
	Extended		85	105		1

1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2 standard.
1. Some applications require operation of LPDDR4 in the maximum temperature conditons in the Elevated Temperature Range be- tween 85°C and 105°C case temperature. For LPDDR4 devices, derating may be neccessary to operate in this range. See MR4 on the section "Mode Register".
2. Either the device case temperature rating or the temperature sensor (See the section of "Temperature Sensor") may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

6. AC and DC Input Measurement Levels

6.1. 1.1V High speed LVCMOS (HS_LLVCMOS)

6.1.1. Standard specifications

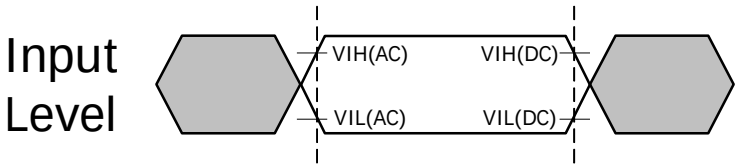
All voltages are referenced to ground except where noted.

Table - LPDDR4 Input level for CKE

Parameter	Symbol	Min	Max	Unit	Notes
Input high level (AC)	VIH(AC)	0.75*VDD2	VDD2+0.2	V	1
Input low level (AC)	VIL(AC)	-0.2	0.25*VDD2	V	1
Input high level (DC)	VIH(DC)	0.65*VDD2	VDD2+0.2	V	
Input low level (DC)	VIL(DC)	-0.2	0.35*VDD2	V	

Notes:
1. Refer to LPDDR4 AC Over/Undershoot section.

Figure - Input AC timing definition for CKE



Note:
1. AC level is guaranteed transition point
2. DC level is hysteresis

6.1.2. LPDDR4 Input Level for Reset_n and ODT_CA

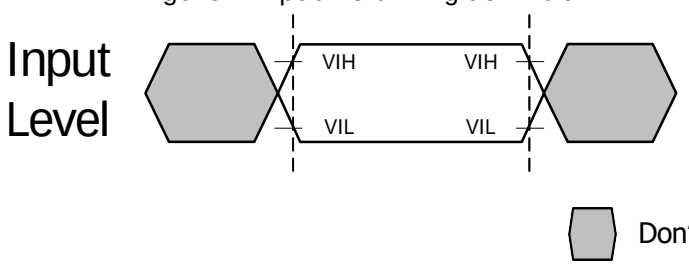
This definition applies to Reset_n and ODT_CA.

Table - LPDDR4 Input level for Reset_n and ODT_CA

Parameter	Symbol	Min	Max	Unit	Notes
Input high level	VIH	0.8*VDD2	VDD2+0.2	V	1
Input low level	VIL	-0.2	0.20*VDD2	V	1

Notes:
1. Refer to LPDDR4 AC Over/Undershoot section.

Figure - Input AC timing definition



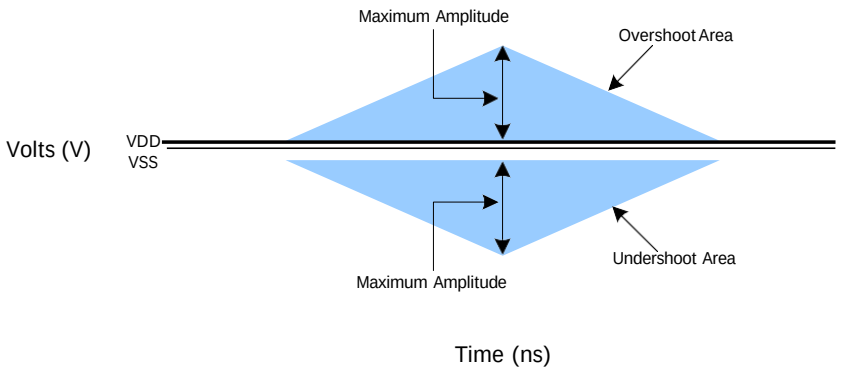
6.1.3. AC Over/Undershoot

6.1.3.1. LPDDR4 AC Over/Undershoot

Table - LPDDR4 AC Over/Undershoot

Parameter	Specification	Units
Maximum peak amplitude allowed for overshoot area	0.3	V
Maximum peak amplitude allowed for undershoot area	0.3	V
Maximum overshoot area above VDD/VDDQ	0.8	V-ns
Maximum undershoot area below VSS/VSSQ	0.8	V-ns

Figure - AC Overshoot and Undershoot Definition for Address and Control Pins



6.2. Differential Input Voltage

6.2.1. Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

Figure - CK Differential Input Voltage

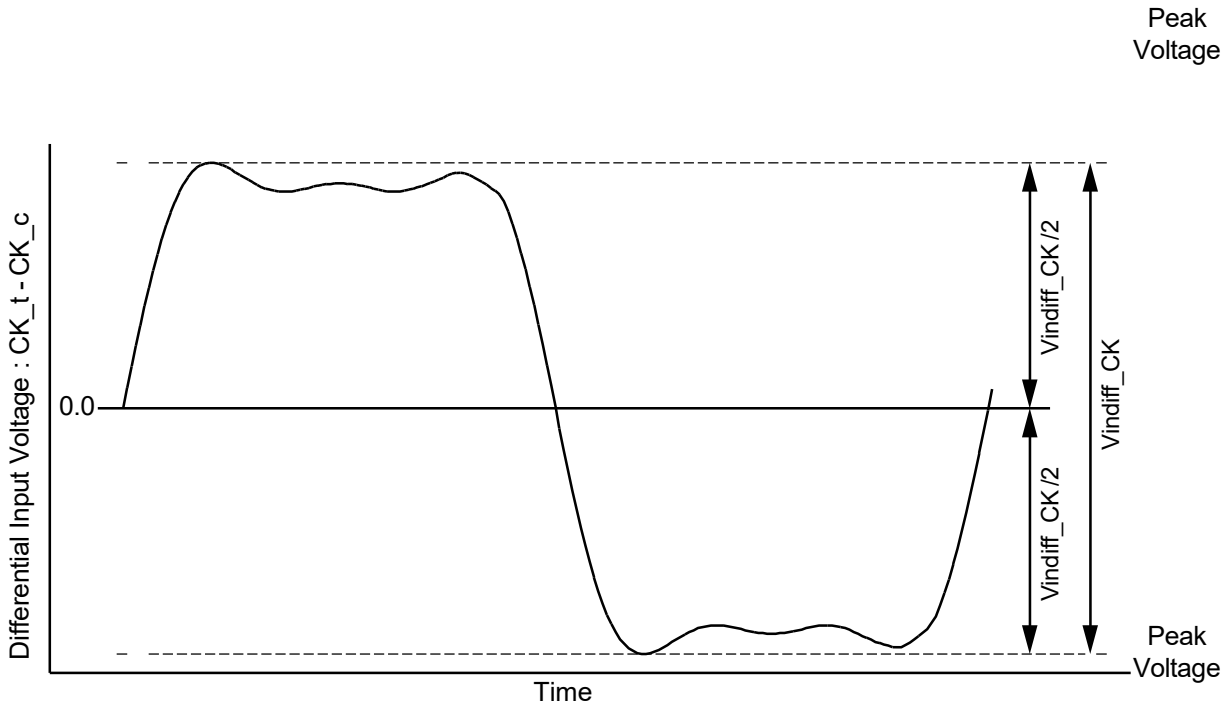


Table - CK differential input voltage

Parameter	Symbol	Data Rate						Unit	Notes
		1600/1867[a]		2133/2400/3200		4266			
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	Vindiff_CK	420	-	380	-	360	-	mV	1

Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VCK_t - VCK_c

a. The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/ 1867.

6.2.2. Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

Figure - DQS Differential Input Voltage

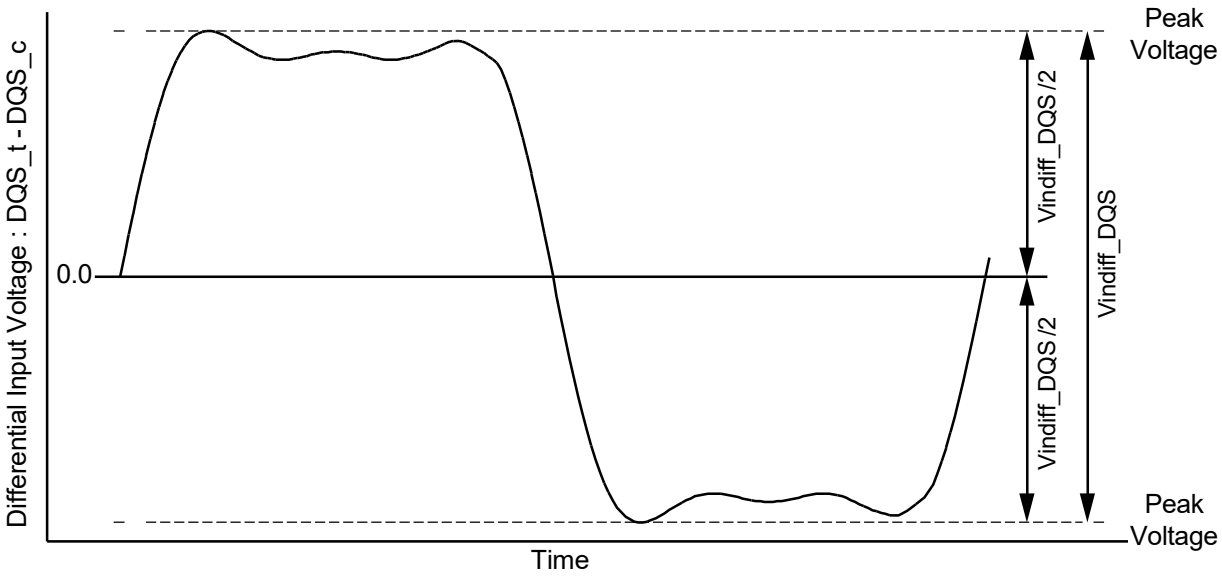


Table - CK differential input voltage

Parameter	Symbol	Data Rate						Unit	Notes
		1600/1867[a]		2133/2400/3200		4266			
		Min	Max	Min	Max	Min	Max		
DQS differential input	Vindiff_DQS	360	-	360	-	340	-	mV	1

Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VDQS_t - VDQS_c

a. The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/ 1867.

6.2.3. Differential Input Cross Point Voltage

Figure - DQS input crosspoint voltage (Vix)

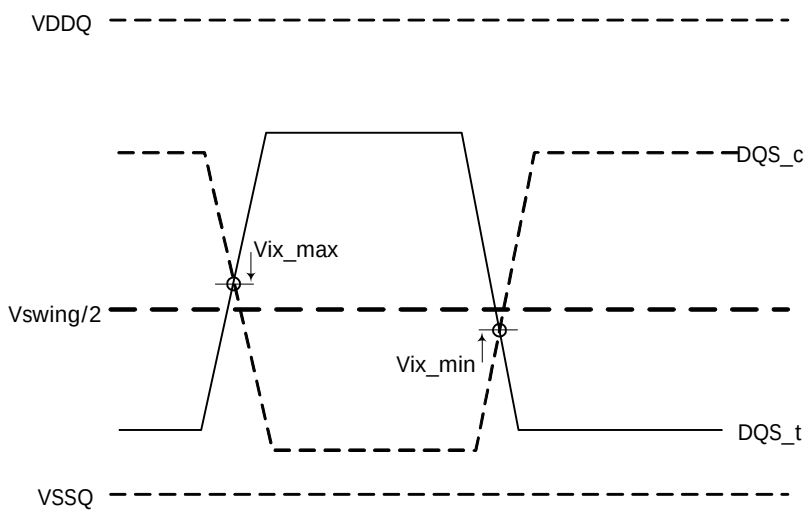


Table - DQS input voltage crosspoint (Vix) ratio

Parameter	Symbol	min/max	LPDDR4 2133	LPDDR4 3200	LPDDR4 4200	Units	Notes
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	max	20	20	20	%	1,2

Notes:
1. The Vix voltage is referenced to Vswing/2(avg)= 0.5(VDQS_t + VDQS_c) where the average is over tbd UI.
2. The ratio of the Vix pk voltage divided by Vdiff_DQS : Vix_DQS_Ratio = 100* (Vix_DQS/Vdiff DQS pk-pk) where VdiffDQS pk-pk = 2*|VDQS_t - VDQS_c|

Figure - CK input crosspoint voltage (Vix)

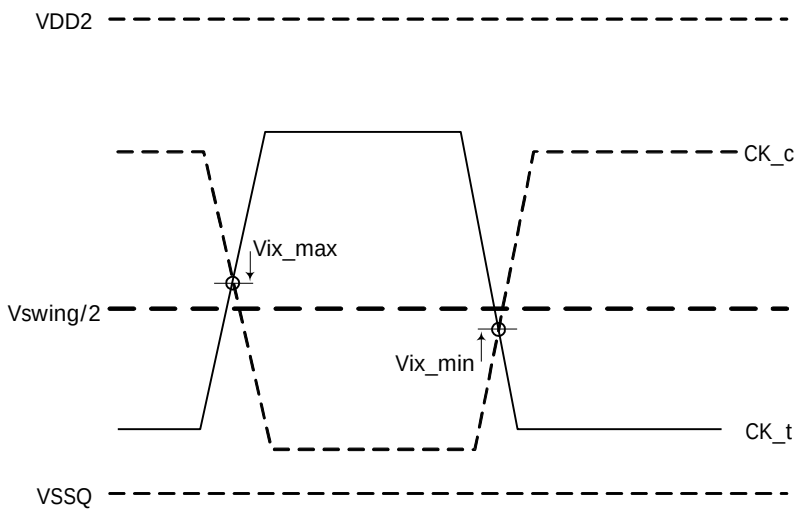


Table - CK input voltage crosspoint (Vix) ratio

Parameter	Symbol	min/max	LPDDR4 2133	LPDDR4 3200	LPDDR4 4200	Units	Notes
CK Differential input crosspoint voltage ratio	Vix_CK_ratio	max	25	25	25	%	1,2

Notes:
1. The Vix voltage is referenced to Vswing/2(avg)= 0.5(VCK_t + VCK_c) where the average is over tbd UI.
2. The ratio of the Vix pk voltage divided by Vdiff_CK : Vix_CK_Ratio = 100* (Vix_CK/Vdiff CK pk-pk) where VdiffCK pk-pk = 2*|VCK_t - VCK_c|

6.3. AC and DC Logic Input Levels for ODT input

Table - LPDDR4 Input level

Parameter	Symbol	Min	Max	Unit	Notes
Input high level (AC)	VIH(AC)	0.75*VDD2	VDD2+0.2	V	1
Input low level (AC)	VIL(AC)	-0.2	0.25*VDD2	V	1
Input high level (DC)	VIH(DC)	0.65*VDD2	VDD2+0.2	V	
Input low level (DC)	VIL(DC)	-0.2	0.35*VDD2	V	

Notes:
1. Refer to LPDDR4 AC Over/Undershoot section.

6.4. Single Ended Output Slew Rate

Figure - Single Ended Output Slew Rate Definition

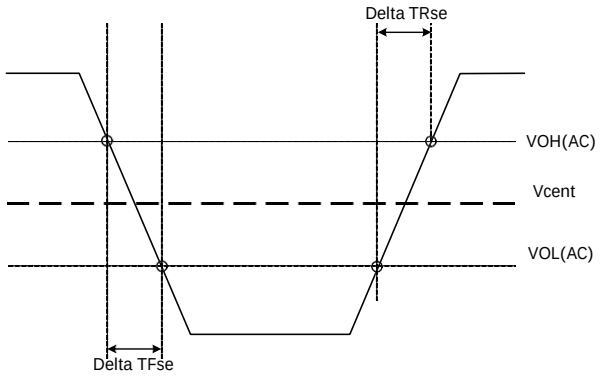


Table - Output Slew Rate (Single-ended)

Parameter	Symbol	Value		Units
		Min (Note 1)	Max (Note 2)	
Single-ended Output Slew Rate (VOH = VDDQ/3)	SRQse	3.5	9.0	V/ns
Output slew-rate matching ratio (Rise to Fall)		0.8	1.2	

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se:
Single-ended Signals

Notes:
1 Measured with output reference load.
2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).
4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

6.5. Differential Output Slew Rate

Figure - Differential Output Slew Rate Definition

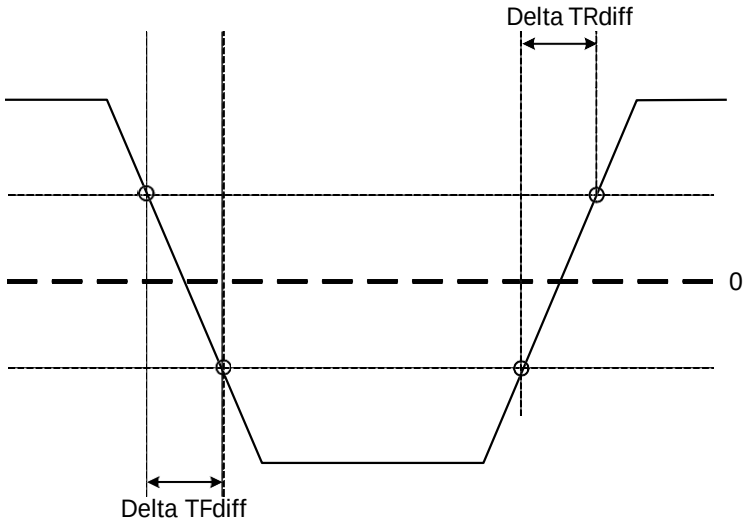


Table - Differential Output Slew Rate

Parameter	Symbol	Value		Units
		Min (Note 1)	Max (Note 2)	
Single-ended Output Slew Rate (VOH = VDDQ/3)	SRQdiff	7	18	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff:
Differential Signals

Notes:
1 Measured with output reference load.
2 The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).
3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

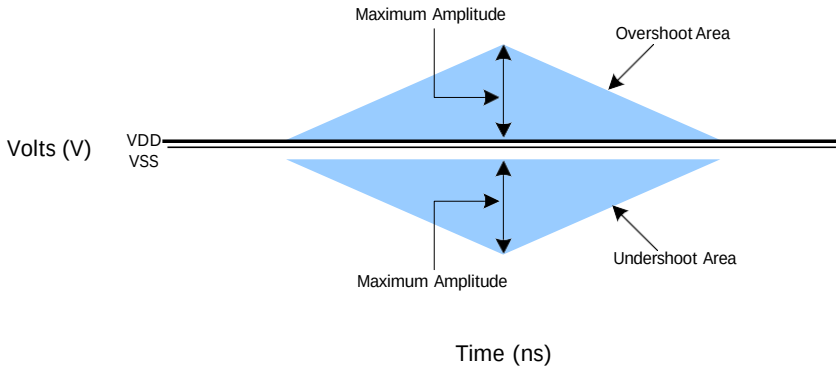
6.6. Overshoot and Undershoot Specification for LVSTL

Table - AC Overshoot / Undershoot Specification

Parameter	1600 to 3200	Units
Maximum peak amplitude allowed for overshoot area	0.3V	V
Maximum peak amplitude allowed for undershoot area	0.3V	V
Maximum overshoot area above VDD/VDDQ	0.1V-ns	V-ns
Maximum undershoot area below VSS/VSSQ	0.1V-ns	V-ns

Notes:
1. VDD stands for VDD2 for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c.
2. VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

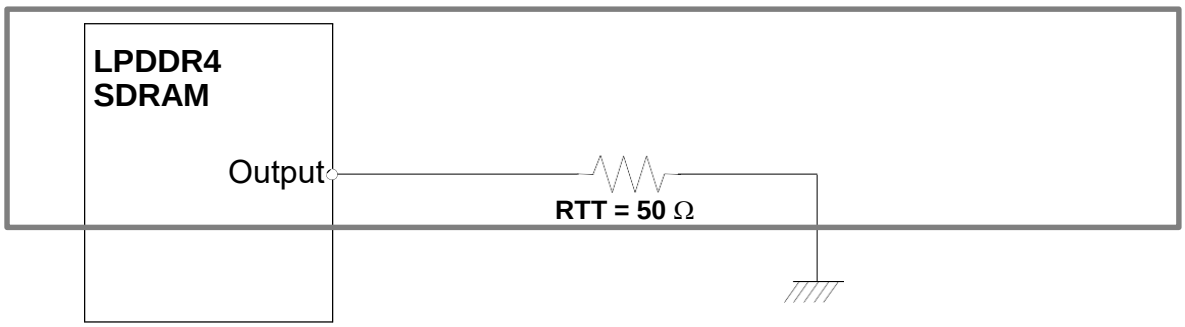
Figure - AC Overshoot and Undershoot Definition



6.7. LVSTL Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure - Driver Output Reference Load for Timing and Slew Rate

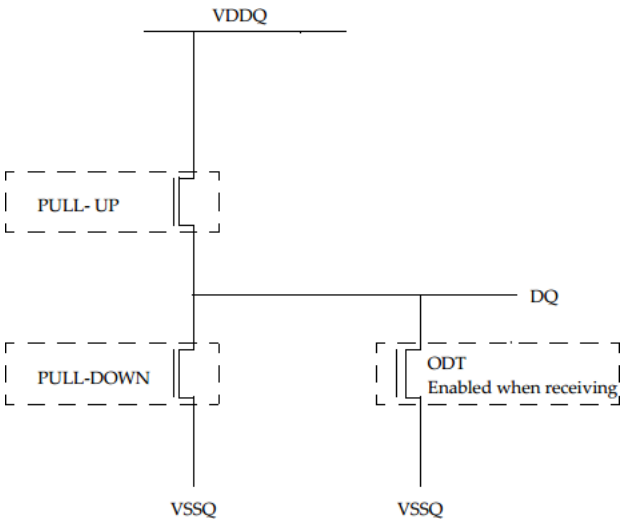


Note: 1. All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

6.8. LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in figure below.

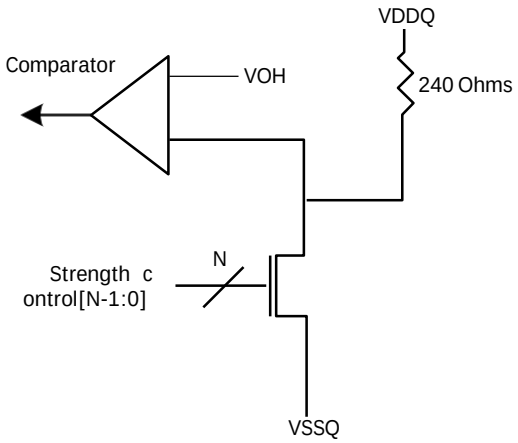
Figure - LVSTL I/O Cell



To ensure that the target impedance is acheived the LVSTL I/O cell is designed to calibrated as following procedure.

1) First calibrate the pull-down device against a 240 Ohm resister to VDDQ via the ZQ pin.
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than VOH.
- NMOS pull-down device is calibrated to 240 Ohms

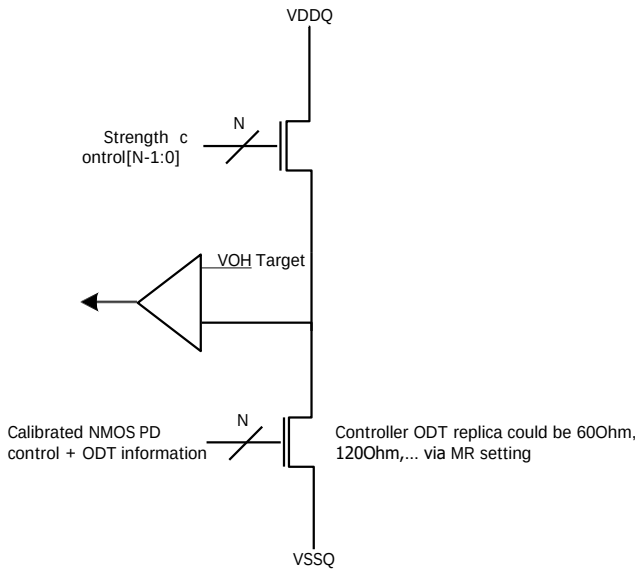
Figure - Pull-down calibration



2) Then calibrate the pull-up device against the calibrated pull-down device.
- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is grater than VOH target
- NMOS pull-up device is now calibrated to VOH target

Figure - Pull-up calibration



7. Input/Output Capacitance

Table - Input/Output Capacitance

Parameter	Symbol	Min/Max	3733-533	Unit	Note
Input capacitance, CK_t and CK_c	CCK	Min	0.5	pF	1,2
		Max	0.9		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	pF	1,2,3
		Max	0.09		
Input capacitance, all other input-only pins	CI	Min	0.5	pF	1,2,4
		Max	0.9		
Input capacitance delta, all other input-only pins	CDI	Min	-0.1	pF	1,2,5
		Max	0.1		
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	Min	0.7	pF	1,2,6
		Max	1.3		
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	Min	0.0	pF	1,2,7
		Max	0.1		
Input/output capacitance delta, DQ and DM	CDIO	Min	-0.1	pF	1,2,8
		Max	0.1		
Input/Output Capacitance ZQ	CZQ	Min	0.0	pF	1,2
		Max	5.0		

Notes

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK_t . CCK_c.
4. CI applieds to CS_n, CKE, CA0~CA5.
5. CDI = CI . 0.5 * (CCK_t + CCK_c)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO . 0.5 * (CDQS_t + CDQS_c) in byte-lane.

8. IDD Specification Parameters and Test Conditions

1. IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: VIN ≤ VIL(DC) MAX

HIGH: VIN ≥ VIH(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See following tables for switching definition of signals.

Table - Definition of switching for CA input signals

Switching for CA								
CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes:
1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table - CA pattern for IDD4R

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	Deselect	L	L	L	L	L	L
N+5	HIGH	LOW	Deselect	L	L	L	L	L	L
N+6	HIGH	LOW	Deselect	L	L	L	L	L	L
N+7	HIGH	LOW	Deselect	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	Deselect	L	L	L	L	L	L
N+13	HIGH	LOW	Deselect	L	L	L	L	L	L
N+14	HIGH	LOW	Deselect	L	L	L	L	L	L
N+15	HIGH	LOW	Deselect	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010, CA[9:4] = 000000 or 111111, Burst Order CA[3:2] = 00 or 11 (Same as LPDDR3 IDD4R Spec)
2. Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.

Table - CA pattern for IDD4W

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	Deselect	L	L	L	L	L	L
N+5	HIGH	LOW	Deselect	L	L	L	L	L	L
N+6	HIGH	LOW	Deselect	L	L	L	L	L	L
N+7	HIGH	LOW	Deselect	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	Deselect	L	L	L	L	L	L
N+13	HIGH	LOW	Deselect	L	L	L	L	L	L
N+14	HIGH	LOW	Deselect	L	L	L	L	L	L
N+15	HIGH	LOW	Deselect	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010, CA[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W Spec.)
2. Difference from LPDDR3 Spec:
   1 No burst ordering
   2 CA pins are kept low with DES CMD to reduce ODT current.

Table - Data Pattern for IDD4W (DBI off)

	DBI OFF case									No. of **1's**
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2

	DBI OFF case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Notes:
1. Simplified pattern compared with last showing.
2. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table - Data Pattern for IDD4R (DBI off)

	DBI OFF case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4

DBI OFF case										No. of **1's**
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Notes:
1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table - Data Pattern for IDD4W (DBI on)

DBI ON case										No. of **1's**
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4

DBI OFF case										No. of **1's**
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

8.2. IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

All values are based on 2 channel.

Table - LPDDR4 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	LPDDR4-2400	Units	Notes
Operating one bank active-precharge current:	$IDD0_1$	VDD1	23.00	mA	
tCK = tCKmin; tRC = tRCmin;	$IDD0_2$	VDD2	52.00	mA	
CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD0_Q$	VDDQ	4.50	mA	3
Idle power-down standby current:	$IDD2P_1$	VDD1	1.30	mA	
tCK =tCKmin;	$IDD2P_2$	VDD2	4.50	mA	
CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD2P_Q$	VDDQ	0.85	mA	3
Idle power-down standby current with clock stop:	$IDD2PS_1$	VDD1	1.30	mA	
CK_t =LOW, CK_c =HIGH;	$IDD2PS_2$	VDD2	4.50	mA	
CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2PS_Q$	VDDQ	0.85	mA	3
Idle non power-down standby current:	$IDD2N_1$	VDD1	3.20	mA	
tCK = CKmin;	$IDD2N_2$	VDD2	26.50	mA	
CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2N_Q$	VDDQ	4.50	mA	3
Idle non power-down standby current with clock stopped:	$IDD2NS_1$	VDD1	3.20	mA	
CK_t=LOW; CK_c=HIGH;	$IDD2NS_2$	VDD2	21.00	mA	
CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2NS_Q$	VDDQ	4.50	mA	3
Active power-down standby current:	$IDD3P_1$	VDD1	6.00	mA	
tCK = CKmin;	$IDD3P_2$	VDD2	6.00	mA	
CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3P_Q$	VDDQ	0.85	mA	3

Parameter/Condition	Symbol	Power Supply	LPDDR4-2400	Units	Notes
Active power-down standby current with clock stop:	$IDD3PS_1$	VDD1	6.00	mA	
CK_t=LOW, CK_c=HIGH;	$IDD3PS_2$	VDD2	6.00	mA	
CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3PS_Q$	VDDQ	0.85	mA	4
Active non-power-down standby current:	$IDD3N_1$	VDD1	12.00	mA	
tCK = tCKmin;	$IDD3N_2$	VDD2	30.00	mA	
CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3N_Q$	VDDQ	4.50	mA	4
Active non-power-down standby current with clock stopped:	$IDD3NS_1$	VDD1	12.00	mA	
CK_t=LOW, CK_c=HIGH;	$IDD3NS_2$	VDD2	22.00	mA	
CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3NS_Q$	VDDQ	4.50	mA	4
Operating burst READ current:	$IDD4R_1$	VDD1	18.00	mA	
tCK = tCKmin;	$IDD4R_2$	VDD2	345.00	mA	
CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_Q$	VDDQ	368.00	mA	5
Operating burst WRITE current:	$IDD4W_1$	VDD1	18.00	mA	
tCK = tCKmin;	$IDD4W_2$	VDD2	370.00	mA	
CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4W_Q$	VDDQ	50.60	mA	4
All-bank REFRESH Burst current:	$IDD5_1$	VDD1	95.00	mA	
tCK = tCKmin;	$IDD5_2$	VDD2	207.00	mA	
CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5_Q$	VDDQ	4.50	mA	4
All-bank REFRESH Average current:	$IDD5AB_1$	VDD1	6.00	mA	
tCK = tCKmin;	$IDD5AB_2$	VDD2	34.00	mA	
CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5AB_Q$	VDDQ	4.50	mA	4

Parameter/Condition	Symbol	Power Supply	LPDDR4-2400	Units	Notes
Per-bank REFRESH Average current:	$IDD5PB_1$	VDD1	6.00	mA	
tCK = tCKmin;	$IDD5PB_2$	VDD2	34.00	mA	
CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5PB_Q$	VDDQ	4.50	mA	4
Self refresh current (85˚C):	$IDD6_1$	VDD1	6.5	mA	6,7,9
CK_t=LOW, CK_c=HIGH;	$IDD6_2$	VDD2	11	mA	6,7,9
CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT disabled	$IDD6_Q$	VDDQ	0.85	mA	4,6,7,9

Notes:
1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. This is the general definition that applies to full array Self Refresh.
7. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated
Temperature Ranges.
8. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
9. IDD6 85oC is guaranteed, IDD6 25/95/105oC is typical of the distribution of the arithmetic mean.
10. IDD6ET is a typical value, is sampled only, and is not tested.

9. Electrical Characteristics and AC Timings

9.1. AC Timing Parameters

Table - Core Parameters

Parameter	Symbol	min max	Data Rate						Unit	Note
			533	1066	1600	2133	2667	3200		
ACTIVE to ACTIVE command period	tRC	min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)						ns	
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)						ns	
Self Refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)						ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 5nCK)						ns	
CAS to CAS delay	tCCD	min	8						tCK(avg)	2
CAS to CAS delay Masked Write w/ECC	tCCDMW	min	4 * tCCD						tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 8nCK)						ns	
RAS to CAS Delay	tRCD	min	max(18ns, 4nCK)						ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns,4nCK)						ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 4nCK)						ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)						ns	
		max	min(9 * tREFI * Refresh Rate, 70.2)						us	3
Write Recovery Time	tWR	min	max{18ns, 4nCK}						ns	
Write to Read Command Delay	tWTR	min	max(10ns, 8nCK)						ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 4ncK)						ns	
Precharge to Precharge Delay	tPPD	min	4						tCK	
Four Bank Activate Window	tFAW	min	40						ns	

Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.
3. Refresh Rate is specified by MR4 OP[2:0].

Table - Clock timings

Parameter	Symbol	min max	LPDDR4 1600	LPDDR4 2400	LPDDR4 3200	Unit	Note
Clock Timing							
Average Clock Period	tCK(avg)	min	1.25	0.833	0.625	ns	
		max	100	100	100		
Average high pulse width	tCH(avg)	min	0.46	0.46	0.46	tCK(avg)	
		max	0.54	0.54	0.54		
Average low pulse width	tCL(avg)	min	0.46	0.46	0.46	tCK(avg)	
		max	0.54	0.54	0.54		
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min			ns	
		max	-				
Absolute clock HIGH pulse width	tCH(abs)	min	0.43	0.43	0.43	tCK(avg)	
		max	0.57	0.57	0.57		
Absolute clock LOW pulse width	tCL(abs)	min	0.43	0.43	0.43	tCK(avg)	
		max	0.57	0.57	0.57		
Clock Period Jitter	tJIT(per)	min	-70	-50	-40	ps	
		max	70	50	40		
Maximum Clock Jitter between two consecutive clock cycles	tJIT(cc)	min	-			ps	
		max	140	100	80		

Table - ZQ Calibration timings

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
ZQ Calibration Time	tZQCAL	max	1						us	
ZQ Calibration Latch Quiet Time	tZQLAT	max	max(30ns, 8nCK)						ns	
Calibration Reset Time	tZQRESET	max	max(50ns, 3nCK)						ns	

Table - DQ Tx Voltage and Timings (Read Timing parameters)

Parameter	Symbol	min max	1600/ 1867	2133/ 2400	3200	Unit	Note
Data Timing							
DQS_t,DQS_c to DQ Skew	tDQSQ	max	0.18			UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min	min(tQSH, tQSL)			UI	1
DQ output window time total, per pin (DBI-Disabled)	tQW_total	min	0.75	0.73	0.7	UI	1,4
DQ output window time deterministic, per pin (DBI-Disabled)	tQW_dj	min	tbd	tbd	tbd	UI	1,4,3
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	max	tbd	tbd	tbd	UI	1
DQ output hold time total from DQS_t, DQS_c (DBI-enabled)	tQH_DBI	min	min(tQSH_DBI, tQSL_DBI)			UI	1
DQ output window time total, per pin (DBI-enabled)	tQW_total_DBI	min	tbd	tbd	tbd	UI	1,4
Read preamble	tRPRE	min	1.8			tCK(avg)	
Read postamble	tRPST	min	0.4			tCK(avg)	
Extended Read postamble	tRPSTE	min	1.4			tCK(avg)	
DQS Low-impedance time from CK_t, CK_c	tLZ(DQS)	min	(RL x tCK) + tDQSCK(Min) - (tPRE(Max) x tCK) - 200ps			ps	
DQS High-impedance time from CK_t, CK_c	tHZ(DQS)	max	(RL x tCK) + tDQSCK(Max) + (RPST(Max) x tCK) - 100ps			ps	
DQ Low-impedance time from CK_t, CK_c	tLZ(DQ)	min	(RL x tCK) + tDQSCK(Min) - 200ps			ps	
DQ High-impedance time from CK_t, CK_c	tHZ(DQ)	max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps			ps	
Data Strobe Timing							
DQS output access time from CK/CK#	tDQSCK	min	1.5			ns	8
		max	3.5				
DQSCK Temperature Drift	tDQSCK_temp	max	4			ps/C	9
DQSCK Volgate Drift	tDQSCK_volt	max	7			ps/mV	10
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	max	1.0			ns	11,12
DQS Output Low Pulse Width (DBI Disabled)	tQSL	min	tCL(abs)-0.05			tCK(avg)	4,5
DQS Output High Pulse Width (DBI Disabled)	tQSH	min	tCH(abs)-0.05			tCK(avg)	4,6
DQS Output Low Pulse Width (DBI Enabled)	tQSL_DBI	min	tCL(abs)-0.045			tCK(avg)	5,7
DQS Output High Pulse Width (DBI Enabled)	tQSH_DBI	min	tCH(abs)-0.045			tCK(avg)	6,7

Notes:

1. DQ to DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
2. The deterministic component of the total timing. Measurement method tbd.
3. This parameter will be characterized and guaranteed by design.
4. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) 0.04.
5. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
6. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
7. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs).
8. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max

voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The volage supply noise must comply to the component Min-Max DC Operating conditions.

9. tDQSCK_temp max delay variation as a function of Temperature.
10. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/ abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.
11. The same voltage and temperature are applied to tDQS2CK_rank2rank.
12. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
13. UI=tCK(avg)min/2

Table - DQ Rx Voltage and Timing Parameters (Write Timing Parameters)

Symbol	Parameter	min max	1600/1867[A)]	2133/2400	3200	Unit	Note
VdIVW_total	Rx Mask voltage p-p total	max	140	140	140	mV	1,2,3,5
VdIVW_dV	Rx Mask voltage - deterministic	max	tbd	tbd	tbd	mV	1,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	max	0.22	0.22	0.25	UI	1,2,4,5
TdIVW_dj	Rx deterministic timing	max	tbd	tbd	tbd	UI	1,5
TdIVW_1bit	Rx timing window 1bit toggle (At VdIVW voltage levels)	max	tbd	tbd	tbd	UI	1,2,4,5 ,14
VIHIL_AC	DQ AC input pulse amplitude p-p	min	180	180	180	mV	7,15
TdIPW	DQ input pulse width (At Vcent_DQ)	min	0.45	0.45	0.45	UI	8
TDQS2DQ	DQ to DQS offset	min	200	200	200	ps	9
		max	800	800	800		
TDQDQ	DQ to DQ offset	max	30	30	30	ps	10
TDQS2DQ_temp	DQ to DQS offset temperature variation	max	0.6	0.6	0.6	ps/^{o}C	11
TDQS2DQ_volt	DQ to DQS offset voltage variation	max	33	33	33	ps/50mV	12
TDQS2DQ_rank2rank	DQ to DQS offset rank to rank	max	200	200	200	ps	17,18
tDQSS	Write command to 1st DQS latching transition	min	0.75			tCK(avg)	
		max	1.25				
tDQSH	DQS input high-level width	min	0.4			tCK(avg)	
tDQSL	DQS input low-level width	min	0.4			tCK(avg)	
tDSS	DQS falling edge to CK setup time	min	0.2			tCK(avg)	
tDSH	DQS falling edge hold time from CK	min	0.2			tCK(avg)	
tWPRE	Write preamble	min	1.8			tCK(avg)	
tWPST	0.5 tCK Write postamble	min	0.4			tCK(avg)	
tWPSTE	1.5 tCK Write postamble	min	1.4			tCK(avg)	
SRIN_dIVW	Input slew rate over VdIVW_total	min	1	1	1	V/ns	13
		max	7	7	7		

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >250KHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels.
5. Defined over the DQ internal Vref range. The Rx mask at the pin must be within the internal Vref DQ range irrespective of the input signal common mode.
6. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd
7. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
8. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
9. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature vari-

ation.

10. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
11. TDQS2DQ max delay variation as a function of temperature.
12. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2.
13. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
14. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
15. VIHL_AC does not have to be met when no transitions are occurring.
16. UI=tCK(avg)min/2
17. The same voltage and temperature are applied to tDQS2DQ_rank2rank
18. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

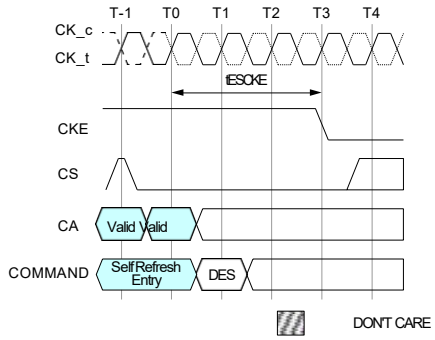
A. The following Rx voltage and timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min/2= 625ps for DQ=1600. For example the TdIVW_total(ps) =0.22*625ps= 137.5ps.

Table - Self-Refresh Timing Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Delay from Self Refresh Entry to CKE Input Low	tESCKE	min	max(1.75ns,3tCK)						nCK	1
Minimum Self-Refresh Time (Entry to Exit)	tSR	min	max(15ns, 3nCK)						ns	1
Self refresh exit to next valid command delay	tXSR	min	max(tRFCab + 7.5ns, 2nCK)						ns	1,2

Note

1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.



2. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are only allowed during this period.

Table - Command Address Input Parameters

Symbol	Parameter	min max	DQ-1333[A)]	DQ-1600/ 1867	DQ-3200	Unit	Note
VcIVW	Rx Mask voltage p-p	max	175	175	155	mV	1,2,4
tcIVW	Rx timing window	max	0.3	0.3	0.3	UI	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	min	210	210	190	mV	5,8
TcIPW	CA input pulse width	min	0.55	0.55	0.6	UI	6
SRIN_cIVW	Input slew rate over VcIVW	min	1	1	1	V/ns	7
		max	7	7	7		

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal Vref range. The Rx mask at the pin must be within the internal Vref CA range irrespective of the input

signal common mode.

5. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
6. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
8. VIHL_AC does not have to be met when no transitions are occurring.
9. UI=tCK(avg)min/2

A. The following Rx voltage and timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. The timing parameters in UI can be converted to absolute time values where tck(avg)min= 1.5ns for DQ=1333. For example the TcIVW(ps) = 0.3*1.5ns=450ps.

Table - Boot Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Clock Cycle Time	tCKb	min	Note 1, 2						ns	
		max	Note 1, 2							
Address & Control Input Setup Time	tISb	min	1150						ps	
Address & Control Input Hold Time	tIHb	min	1150						ps	
DQS Output Data Access Time from CK/CK#	tDQSCKb	min	2						ns	
		max	10							
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb	max	1.2						ns	

Notes

1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

Table - Mode Register Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Additional time after tXP has expired until the MRR command may be issued	tMRRI	min	tRCD + 3nCK						ns	
MODE REGISTER Write command period	tMRW	min	max(10ns, 10nCK)						ns	
MODE REGISTER Read command period	tMRR	min	8						nCK	
Mode Register Write Set Command Delay	tMRD	min	max(14ns, 10nCK)						ns	

Table - VRCG Enable/Disable Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
VREF high current mode enable time	tVRCG_Enable	max	200						ns	
VREF high current mode disable time	tVRCG_Disable	max	100						ns	

Table - Command Bus Training Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Valid Clock Requirement after CKE Input Low	tCKELCK	min	max(5ns, 5nCK)						-	
Data Setup for Vref Training Mode	tDStrain	min	2						ns	
Data Hold for Vref Training Mode	tDHtrain	min	2						ns	
Asynchronous Data Read	tADR	max	20						ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	min	RU(tADR/tCK)						tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	min	10						ns	1
First CA Bus Training Command Following CKE Low	tCAENT	min	250						ns	

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Vref Step Time – multiple steps	tVref_long	max	250						ns	
Vref Step Time – one step	tVref_short	max	80						ns	
Valid Clock Requirement before CS High	tCKPRECS	min	2*tCK + tXP						-	
Valid Clock Requirement after CS High	tCKPSTCS	min	max (7.5ns, 5nCK)						-	
Minimum delay from CS to DQS toggle in command bus training	tCS_Vref	min	2						tCK	
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	min	10						ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	min	max(1.75ns, 3nCK)						-	
CA Bus Training CKE High to DQ Tri-state	tMRZ	min	1.5						ns	
ODT turn-on latency from CKE	tCKELODTon	min	20						ns	
ODT turn-off latency from CKE	tCKELODToff	min	20						ns	

Notes:
1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

Table - Write Leveling Parameters

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	min	20						tCK	
Write preamble for Write Leveling	tWLWPRE	min	20						tCK	
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	min	40						tCK	
Write leveling output delay	tWLO	min	0						ns	
		max	20							
Valid Clock Requirement before DQS Toggle	tCKPRDQS	min	max(7.5ns, 4nCK)							
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	min	max(7.5ns, 4nCK)							
Write leveling hold time	tWLH	min			150	100		75	ps	1,2
Write leveling setup time	tWLS	min			150	100		75	ps	1,2
Write leveling invalid window	tWLIVW_Total	min			240	160		120	ps	1,2

Notes:
1. In addition to the traditional setup and hold time specifications above, there is value in a invalid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW_Total is defined in a similar manner to tdIVW_Total, except that here it is a DQS invalid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling invalid window.

   The DQS input mask for timing with respect to CK is shown in the following figure. The "total" mask (TdiVW_total) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

Figure - DQS_t/DQS_c and CK_t/CK_c at DRAM Latch

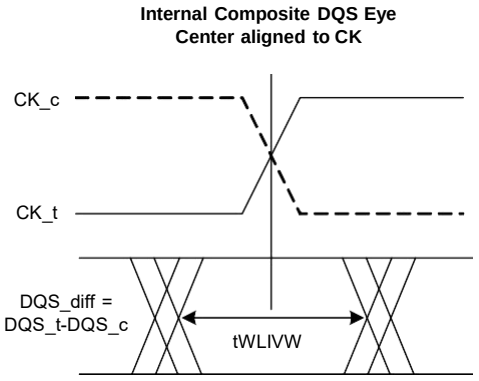


Table - Read Preamble Training Timings

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Delay from MRW command to DQS Driven out	tSDO	max	min(tMRD, 15ns)						tCK	1

Table - MPC [Write FIFO] AC Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Additional time after tXP has expired until MPC [Write FIFO] command may be issued	tMPCWR	min	tRCD + 3nCK							

Table - DQS Interval Oscillator AC Timing

Parameter	Symbol	min max	Value	Unit	Note
Delay time from OSC stop to Mode Register Readout	tOSCO	min	max(40ns,8nCK)	ns	

Table - Frequency Set Point Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
Frequency Set Point Switching Time	tFC_Short	min	200						ns	1
	tFC_Middle	min	200						ns	1
	tFC_Long	min	250						ns	1
Valid Clock Requirement after entering FSP change	tCKFSPE	min	max(7.5ns, 4nCK)							
Valid Clock Requirement before 1st valid command after FSP change	tCKFSPX	min	max(7.5ns, 4nCK)							

Notes:
1. Frequency Set Point Switching Time depends on value of Vref(ca) setting: MR12 OP[5:0] and Vref(ca) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table "tFC value maping".
   Additionally change of Frequency Set Point may affect Vref(dq) setting. Setting time of Vref(dq) level is same as Vref(ca) level.

Table - CA ODT setting timing

Parameter	Symbol	Min/Max	LPDDR4-1600/1866/2133/2400/3200	Units	Note
ODT CA Value Update Time	tODTUP	Min	RU(tbd ns/tCK(avg))		

Table - Power Down Timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	min	Max(7.5ns,4nCK)						-	
Delay from valid command to CKE input LOW	tCMDCKE	min	Max(1.75ns,3nCK)						ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	min	Max(5ns,5nCK)						ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	min	1.75						ns	
Valid CS Requirement after CKE Input low	tCKELCS	min	Max(5ns, 5nCK)						ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	min	Max(1.75ns, 3nCK)						ns	1
Exit power- down to next valid command delay	tXP	min	Max(7.5ns, 5nCK)						ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	min	1.75						ns	
Valid CS Requirement after CKE Input High	tCKEHCS	min	Max(7.5ns, 5nCK)						ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	min	Max(14ns, 10nCK)						ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	min	Max(1.75ns, 3nCK)						ns	1

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).
   For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 3.75ns has transpired. The case which 3nCK is applied to is shown below.

Figure - tCMDCKE Timing

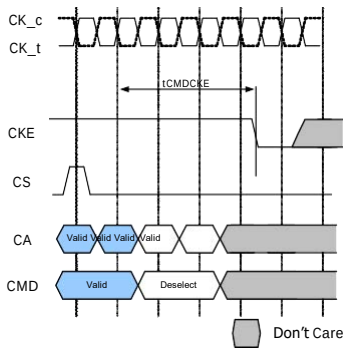


Table - PPR Timing Parameters

Parameter	Symbol	LPDDR4		Unit	Notes
		Min	Max		
PPR Programming Time	tPGM	1000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting Time	tPGMPST	50	-	us	

Table - Temperature Derating for AC timing

Parameter	Symbol	min max	DDR4 533	DDR4 1066	DDR4 1600	DDR4 2133	DDR4 2667	DDR4 3200	Unit	Note
DQS Output access time from CK_t/CK_c (derated)	tDQSCKd	max	3600						ps	1
RAS-to-CAS delay (derated)	tRCDd	min	tRCD + 1.875						ns	1
Activate-to-Activate command period (derated)	tRCd	min	tRC + 3.75						ns	1
Row active time (derated)	tRASd	min	tRAS + 1.875						ns	1
Row precharge time (derated)	tRPd	min	tRP + 1.875						ns	1
Active bank A to Active bank B (derated)	tRRDd	min	tRRD + 1.875						ns	1

Notes:
1. Timing derating applies for operation at 85ºC to 105ºC

9.2. CA Rx voltage and timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be e xpected to be able to successfully capture a valid input signal; it is not the valid data-eye.

Figure - CA Receiver(Rx) mask

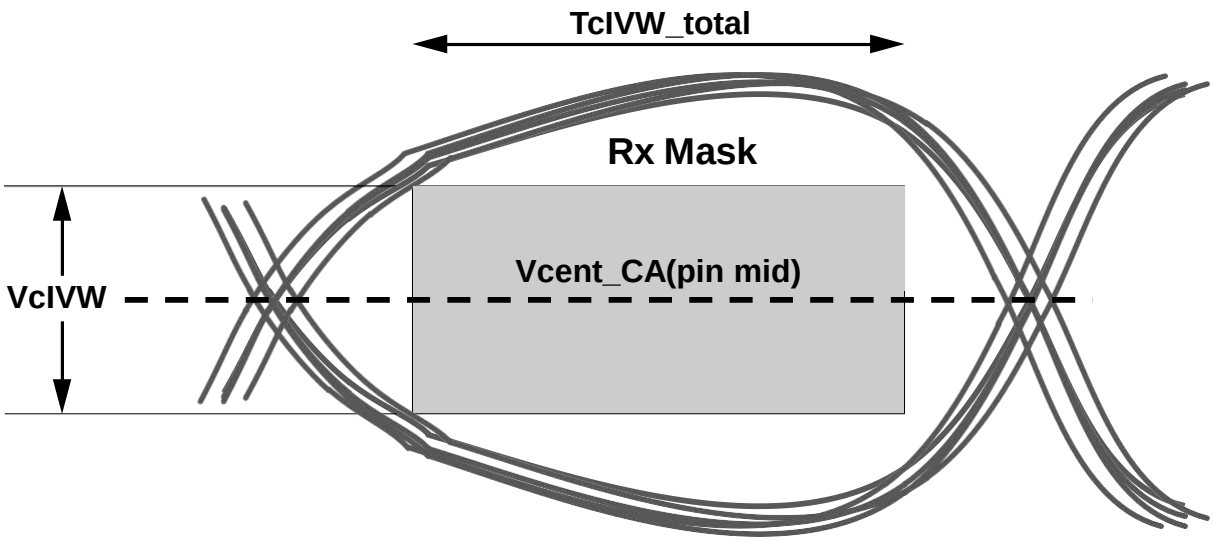
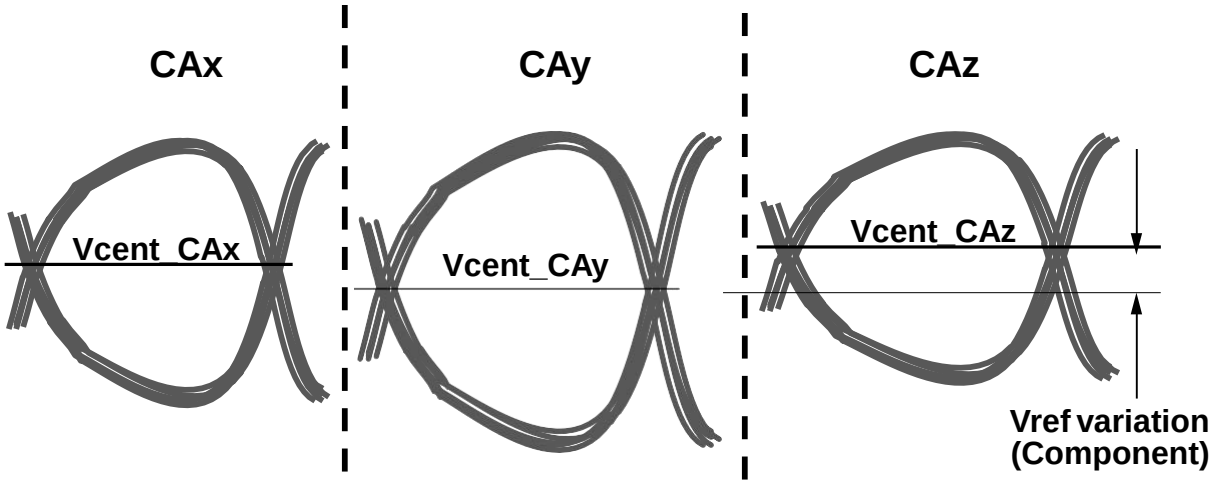


Figure - Across pin Vref CA voltage variation

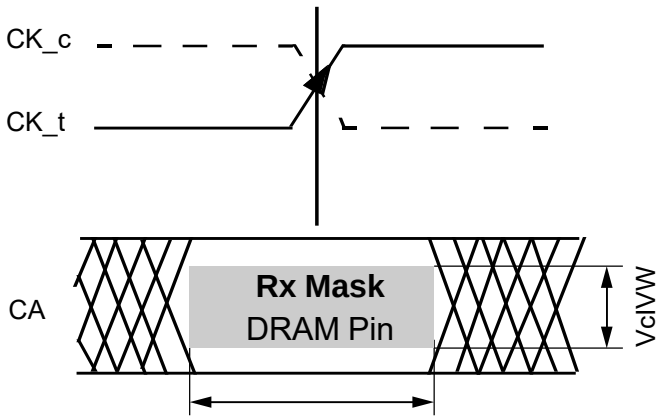


Vcent_CA(pin avg) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA pin Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in the above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask.The component level Vref will be set by the

system to account for Ron and ODT settings.

Figure - CA Timing at the DRAM pins

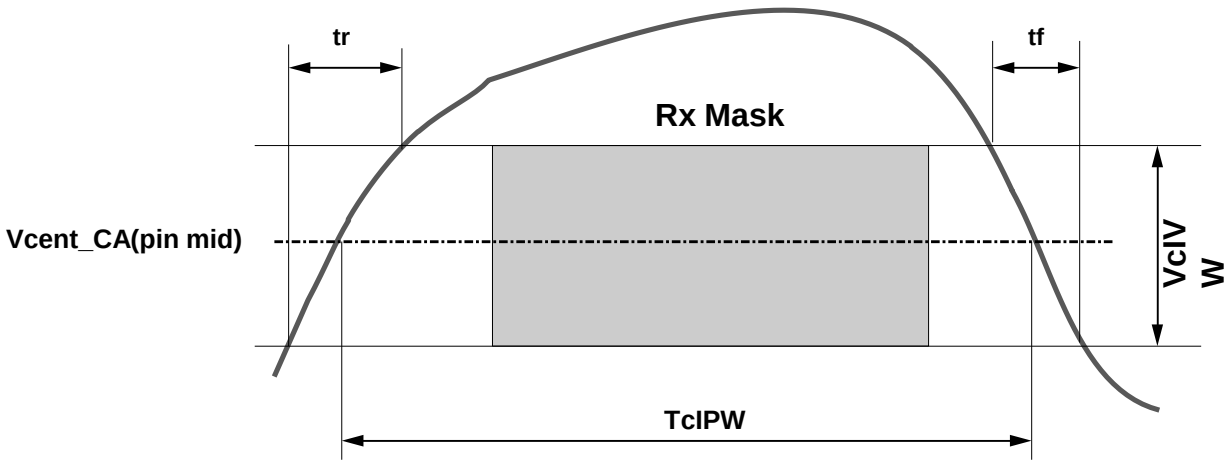
CK_t, CK_c Data-in at DRAM Pin Minimum CA Eye center aligned



TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

All of the timing terms in figure 150 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

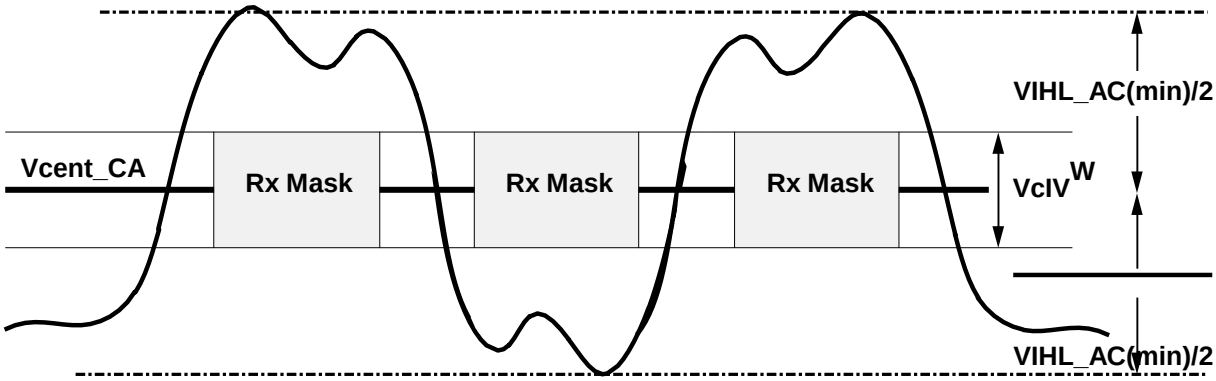
Figure - CA TcIPW and SRIN_cIVW definition (for each input pulse)



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Notes:
1. SRIN_cIVW=VcIVW/(tr or tf), signal must be monotonic within tr and tf range.

Figure - CA VIHIL_AC definition (for each input pulse)



9.3. DRAM Data Timing

Figure - Read data timing definitions tQH and tDQSQ across on DQ signals per DQS group

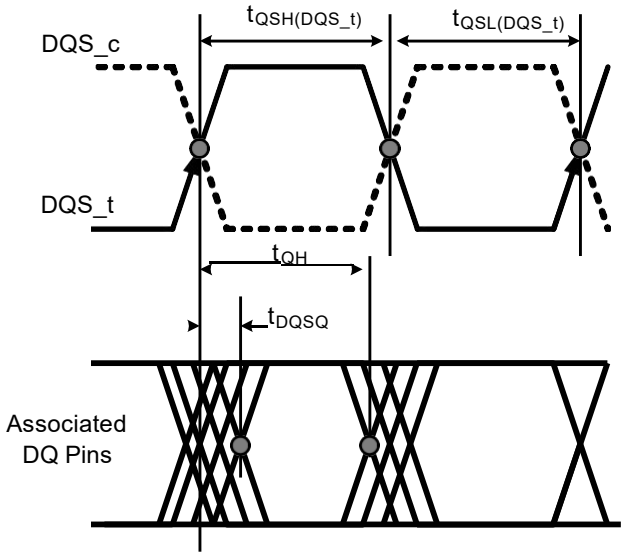
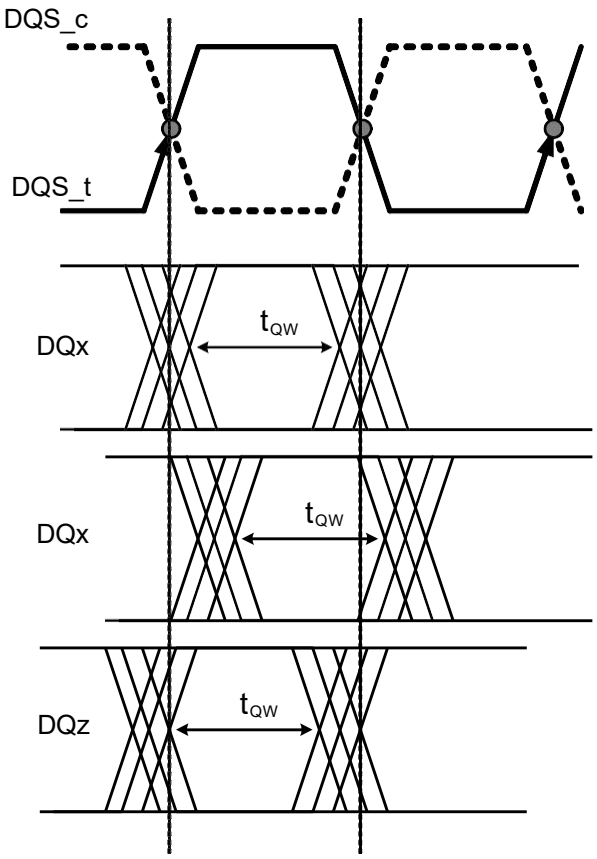


Figure - Read data timing tQW valid window defined per DQ signal



9.4. DQ Rx Voltage and Timing Definition

The DQ input receiver mask for voltage and timing is shown in figure below, is applied per pin. The "total" mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.

Figure - DQ Receiver(Rx) mask

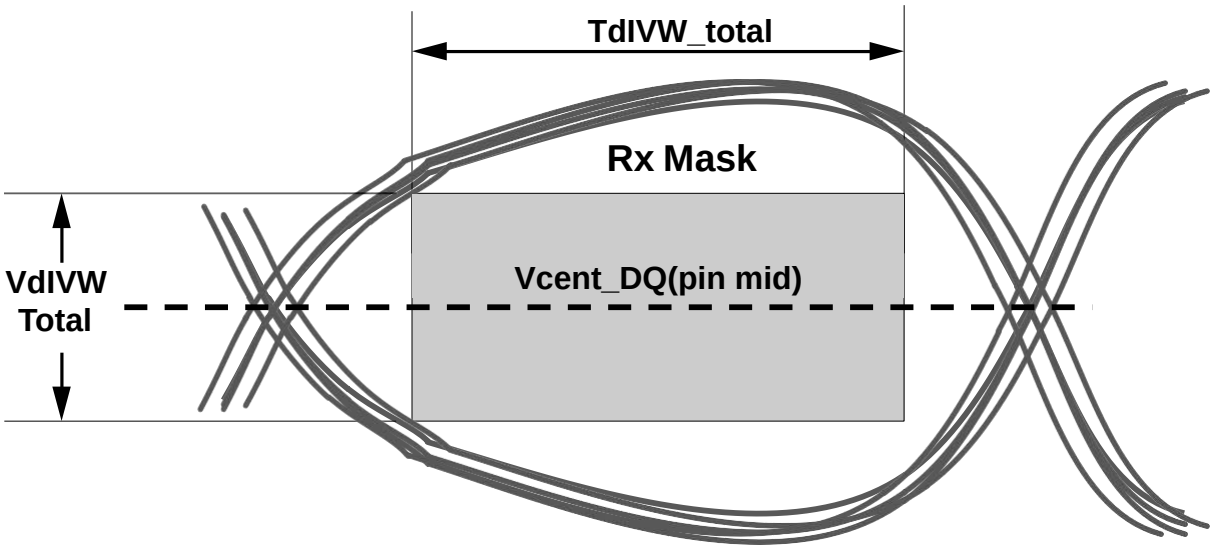
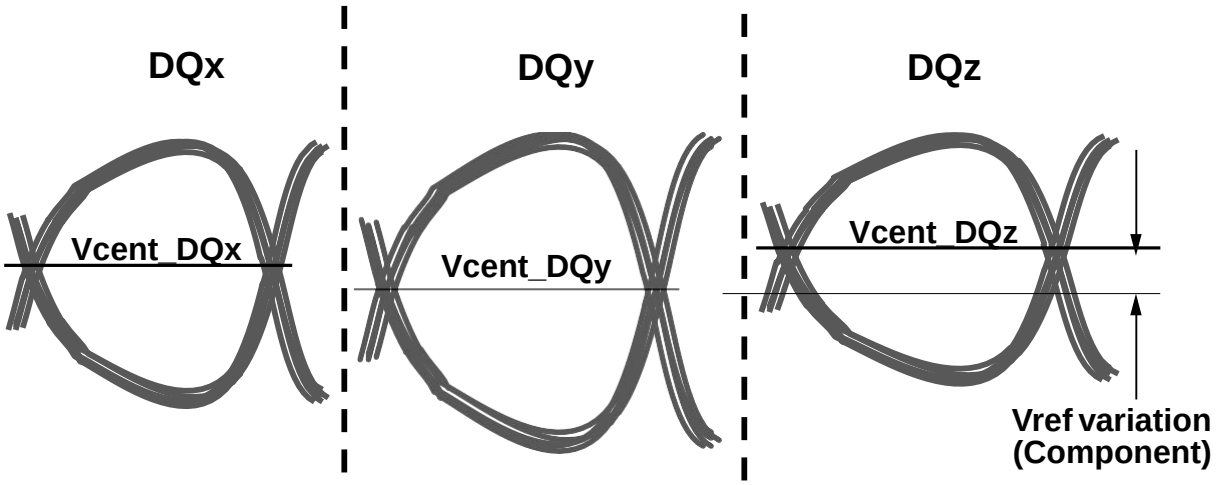
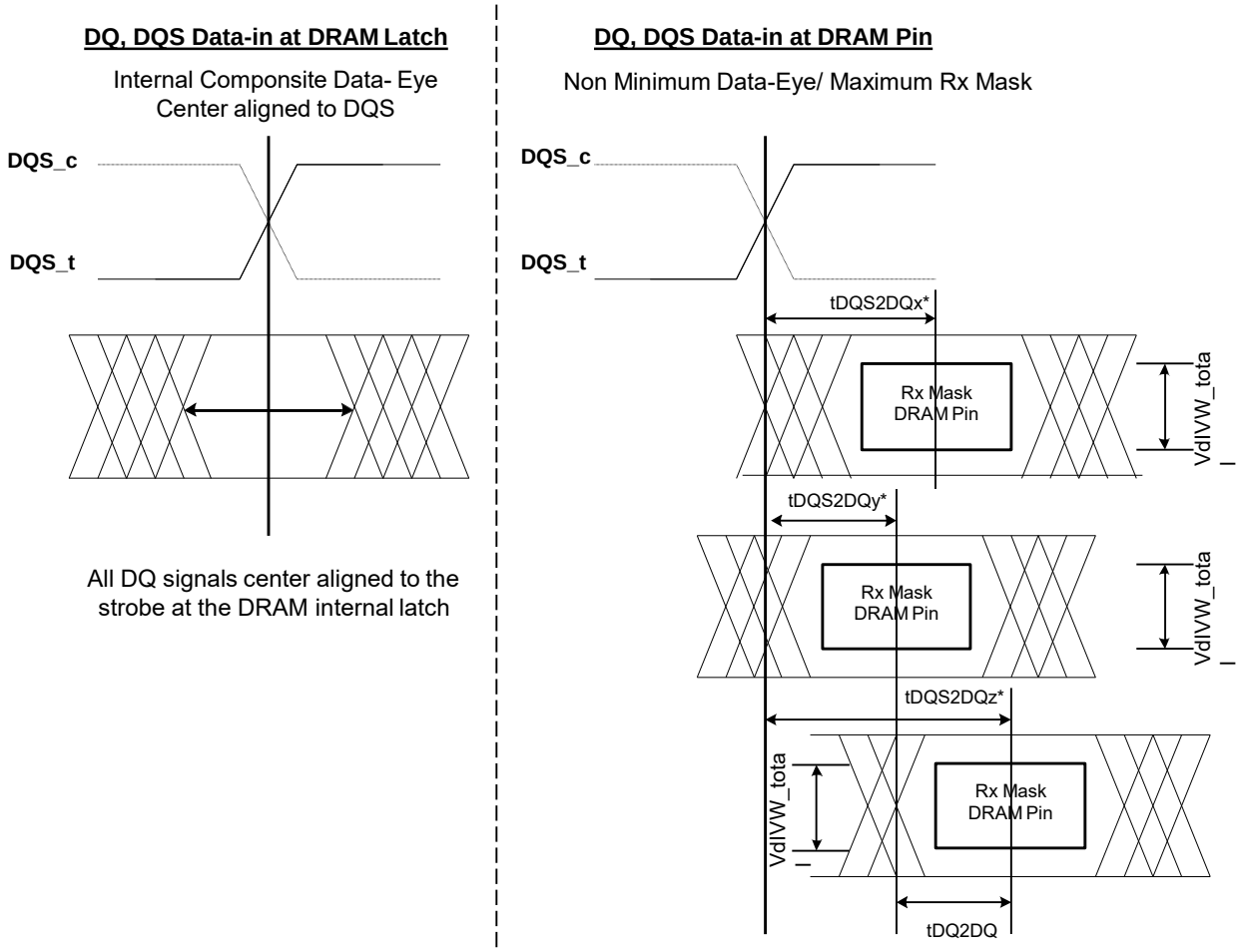


Figure - Across pin Vref DQ voltage variation



Vcent_DQ(pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in the above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.

Figure - DQ to DQS (tDQS2DQ and tDQDQ) Timings at the DRAM pins referenced from the internal latch

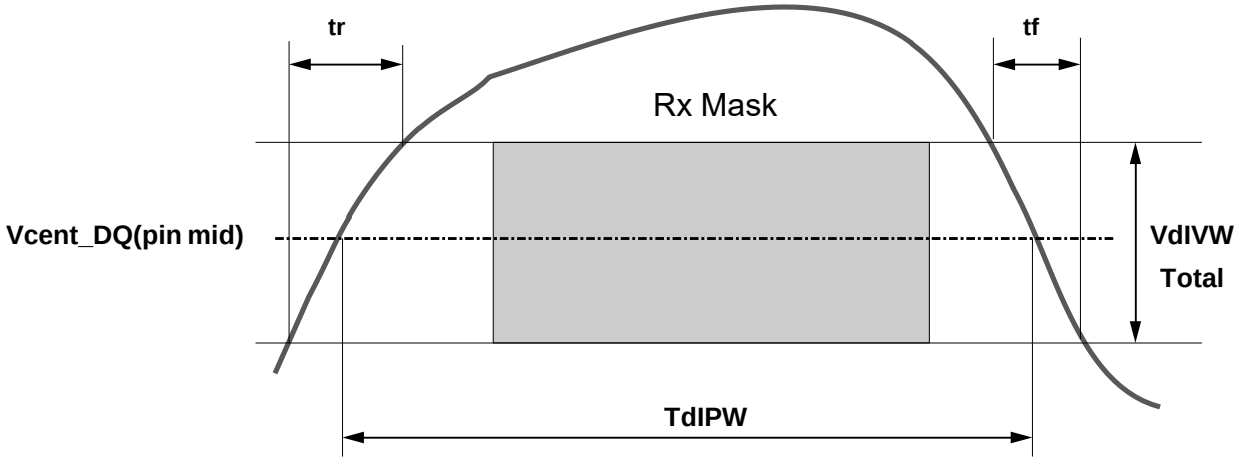


NOTE:

1. tDQS2DQ is measured at the center(midpoint) of the TdiVW window.
2. DQz represents the max tDQS2DQ in this example
3. DQy represents the min tDQS2DQ in this example

All of the timing terms in DQ to DQS t are measured from the DQS_t/DQS_c to the center(midpoint) of the TdIVW window taken at the VdIVW_total voltage levels centered around Vcent_DQ(pin_mid). In the above figure the timings at the pins are referenced with respect to all DQ signals center aligned to the DRAM internal latch. The data to data offset is defined as the difference between the min and max tDQS2DQ for a given component.

Figure - DQ TdIPW and SRIN_dIVW definition (for each input pulse)



Note
1. SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Notes:
1. SRIN_dIVW-VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure - DQ VIHL_AC definition (for each input pulse)